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H4P PAL

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GB 2334836 A
EP 0880250 A1
EP 0817418 A1
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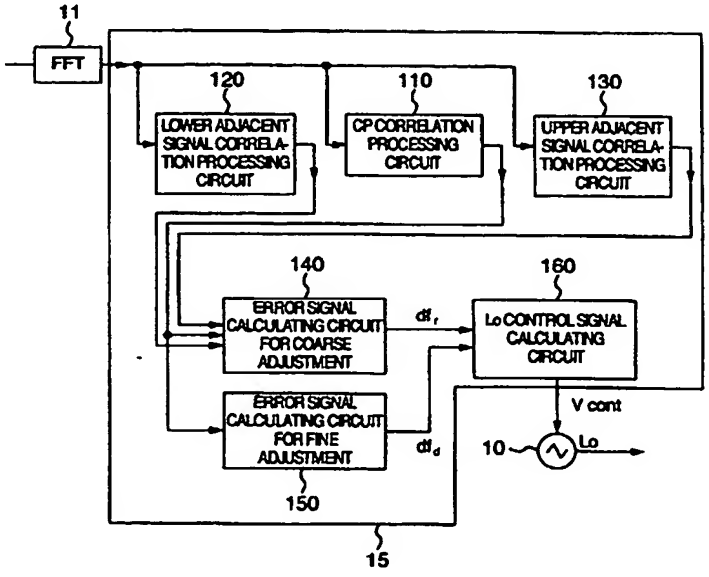
ONLINE : EPODOC, WPI, JAPIO

(54) Abstract Title
OFDM RECEIVERS

(57) A signal transmission system of orthogonal frequency division multiplexing having a transmitting apparatus and a receiving apparatus to transmit OFDM signal. The receiving apparatus according to the invention comprises; an input portion having an antenna (8), a mixer (9) and a local oscillator (10), for receiving the OFDM signal from the transmitting apparatus; a first Fourier transforming circuit (11) coupled with the input portion to convert the OFDM signal into base-band signals having a plurality of carriers with a symbol frequency and a predetermined symbol period, said carriers including pilot signals; a demodulation unit (13) coupled with the fast Fourier transforming circuit (11), for decoding to be produced as information codes; and a pilot signal correlation processing unit (15) coupled with the local oscillator (10) and the fast Fourier transforming circuit, for calculating a correlation value relating to the pilot signal, and controlling a frequency of the local oscillator based on the result of calculation of the correlation value.

FIG.1



GB 2 368 250 A

FIG.1

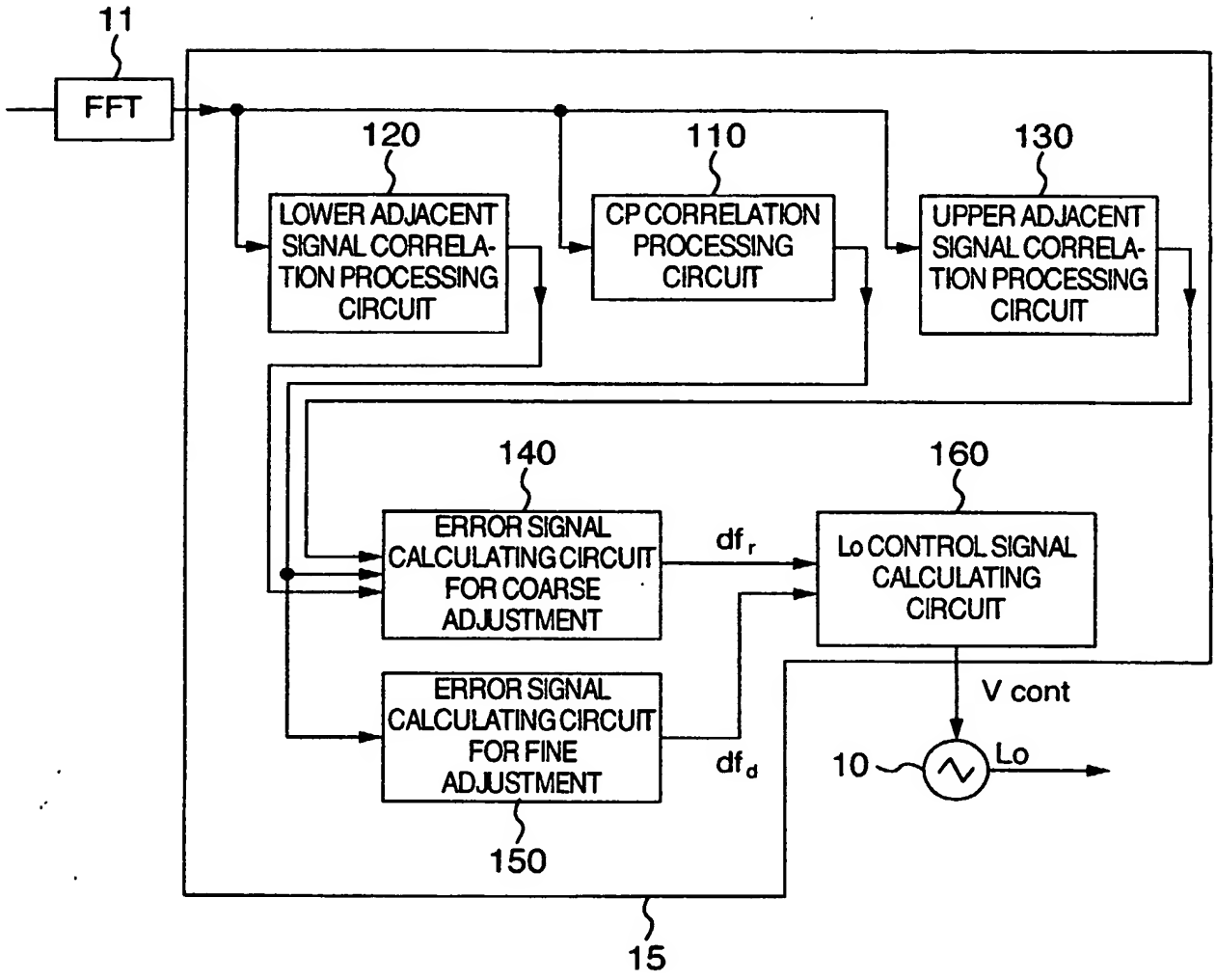

11
FFT
120
LOWER ADJACENT SIGNAL CORRELATION PROCESSING CIRCUIT
110
CP CORRELATION PROCESSING CIRCUIT
130
UPPER ADJACENT SIGNAL CORRELATION PROCESSING CIRCUIT
140
ERROR SIGNAL CALCULATING CIRCUIT FOR COARSE ADJUSTMENT
df_r
160
Lo CONTROL SIGNAL CALCULATING CIRCUIT
ERROR SIGNAL CALCULATING CIRCUIT FOR FINE ADJUSTMENT
df_d
V cont
10
Lo
150
15

FIG.2

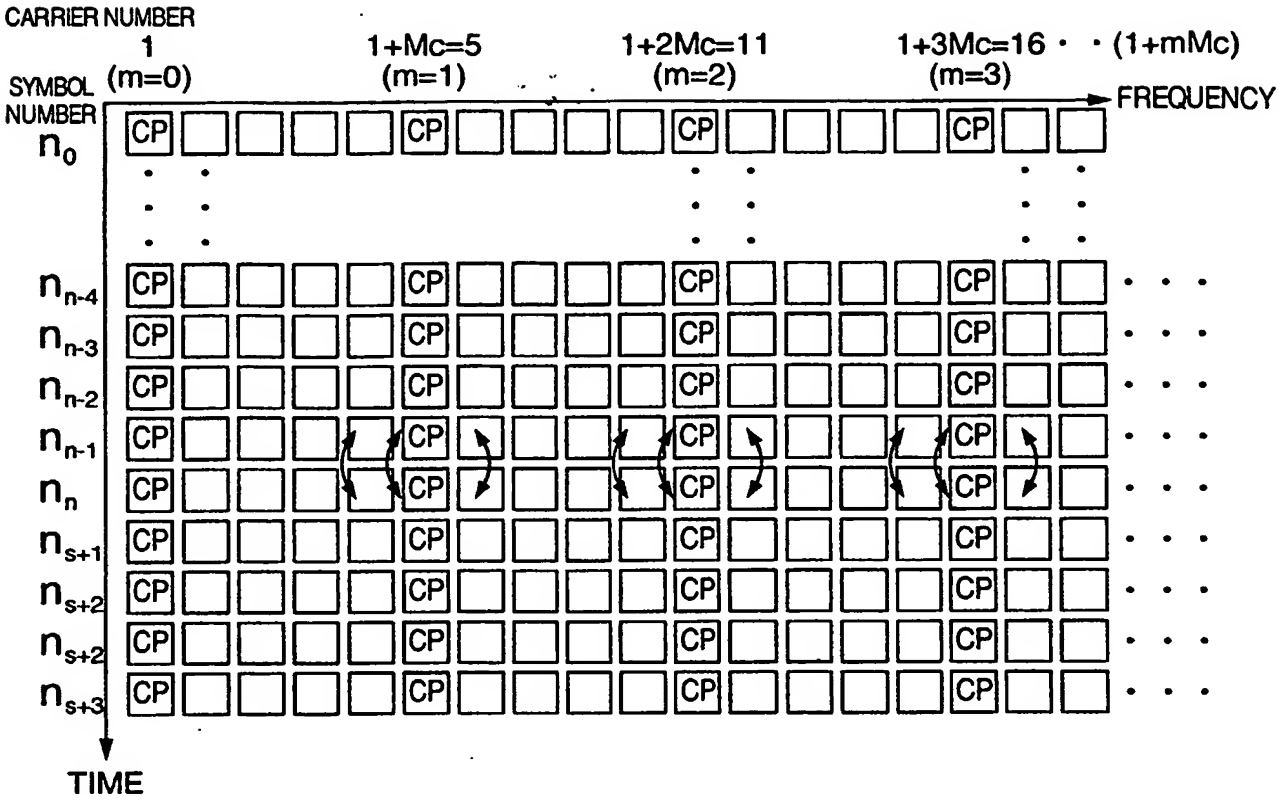

CARRIER NUMBER
1 (m=0)
1+Mc=5 (m=1)
1+2Mc=11 (m=2)
1+3Mc=16 · · (1+mMc)
SYMBOL NUMBER
FREQUENCY
CP
n_0
n_{n-4}
n_{n-3}
n_{n-2}
n_{n-1}
n_n
n_{s+1}
n_{s+2}
n_{s+2}
n_{s+3}
TIME

FIG.3

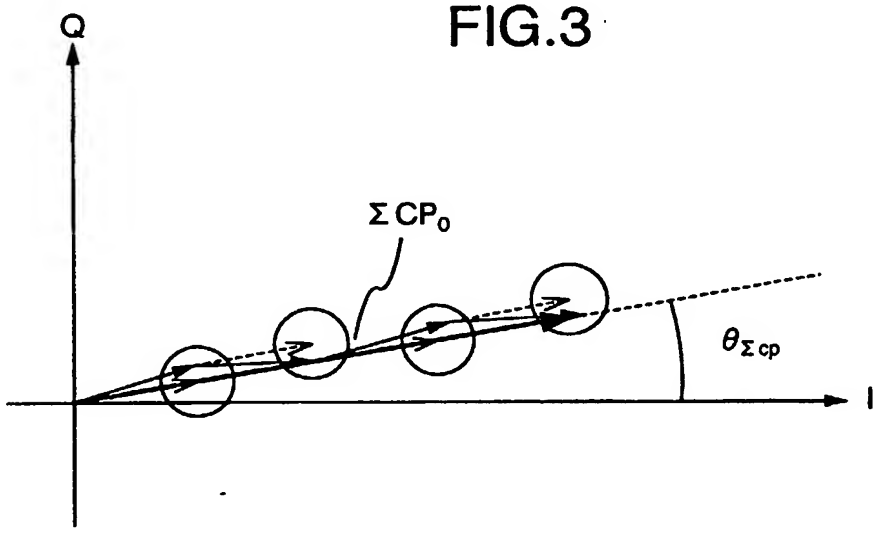

Q
ΣCP_0
$\theta_{\Sigma cp}$
I

FIG.4

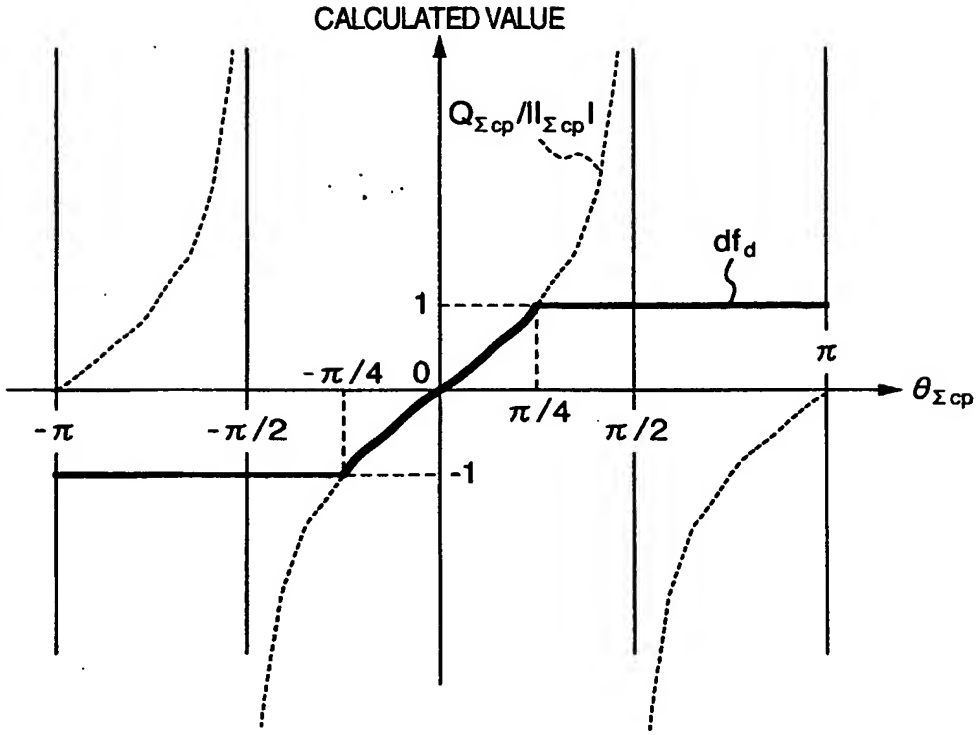

CALCULATED VALUE
$Q_{\Sigma cp}/|I_{\Sigma cp}|$
df_d
1
-1
$-\pi$
$-\pi/2$
$-\pi/4$
0
$\pi/4$
$\pi/2$
π
$\theta_{\Sigma cp}$

FIG.5

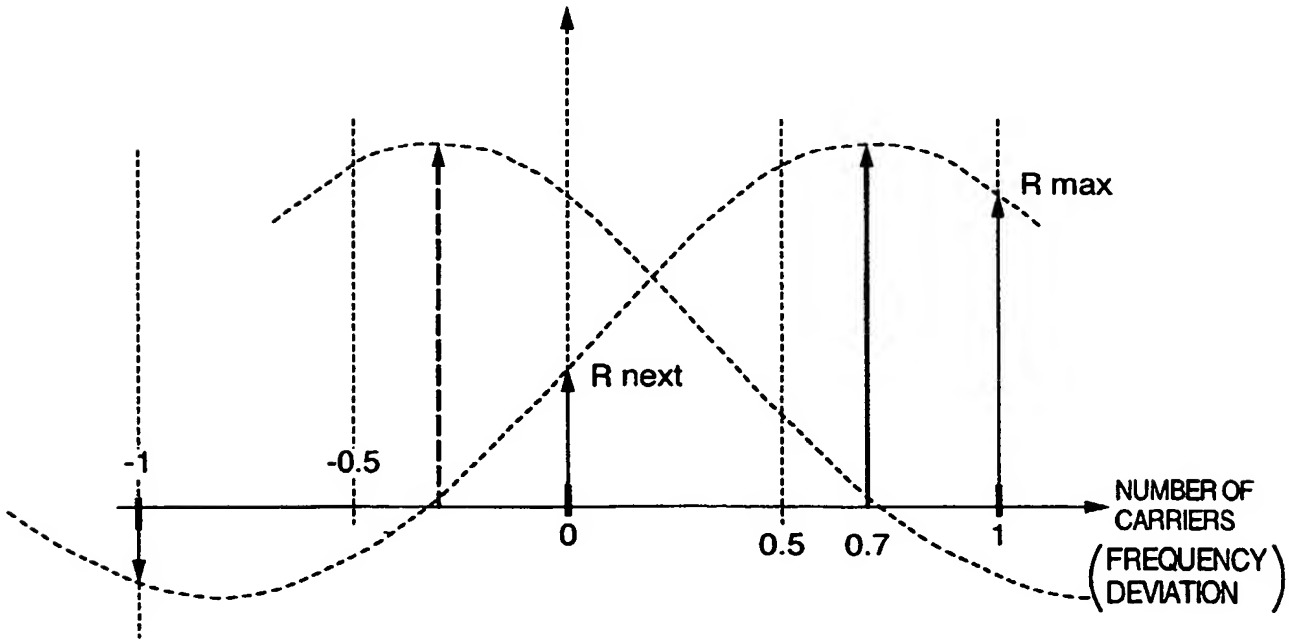

R max
R next
-1
-0.5
0
0.5
0.7
1
NUMBER OF CARRIERS
(FREQUENCY DEVIATION)

FIG.6

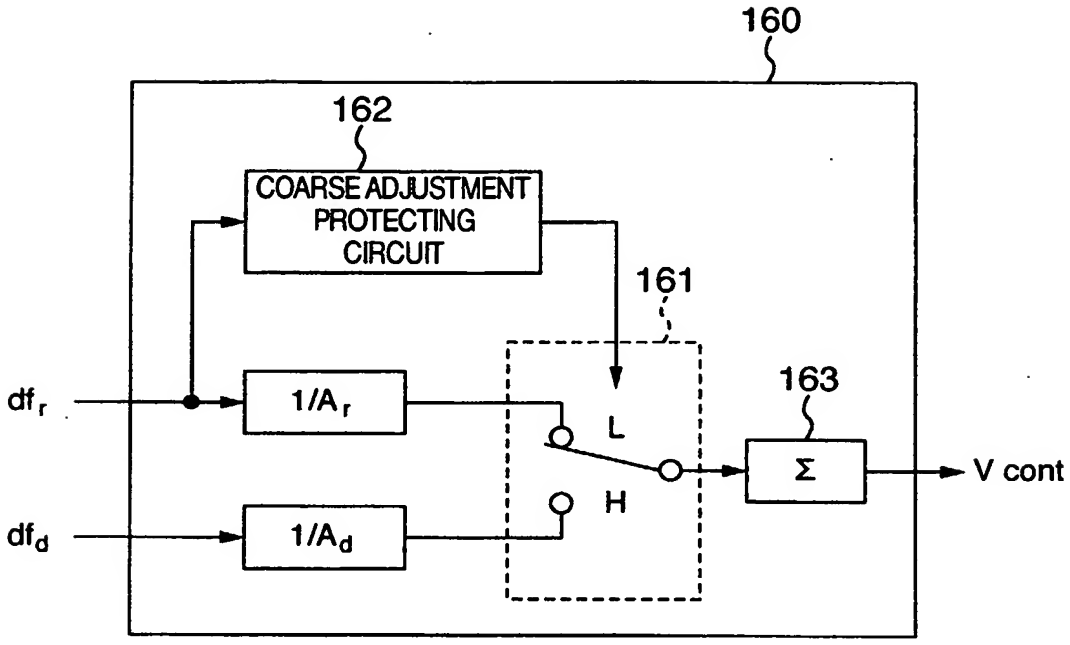

160
162
COARSE ADJUSTMENT PROTECTING CIRCUIT
161
163
df_r
1/A_r
L
Σ
V cont
df_d
1/A_d
H

FIG.7

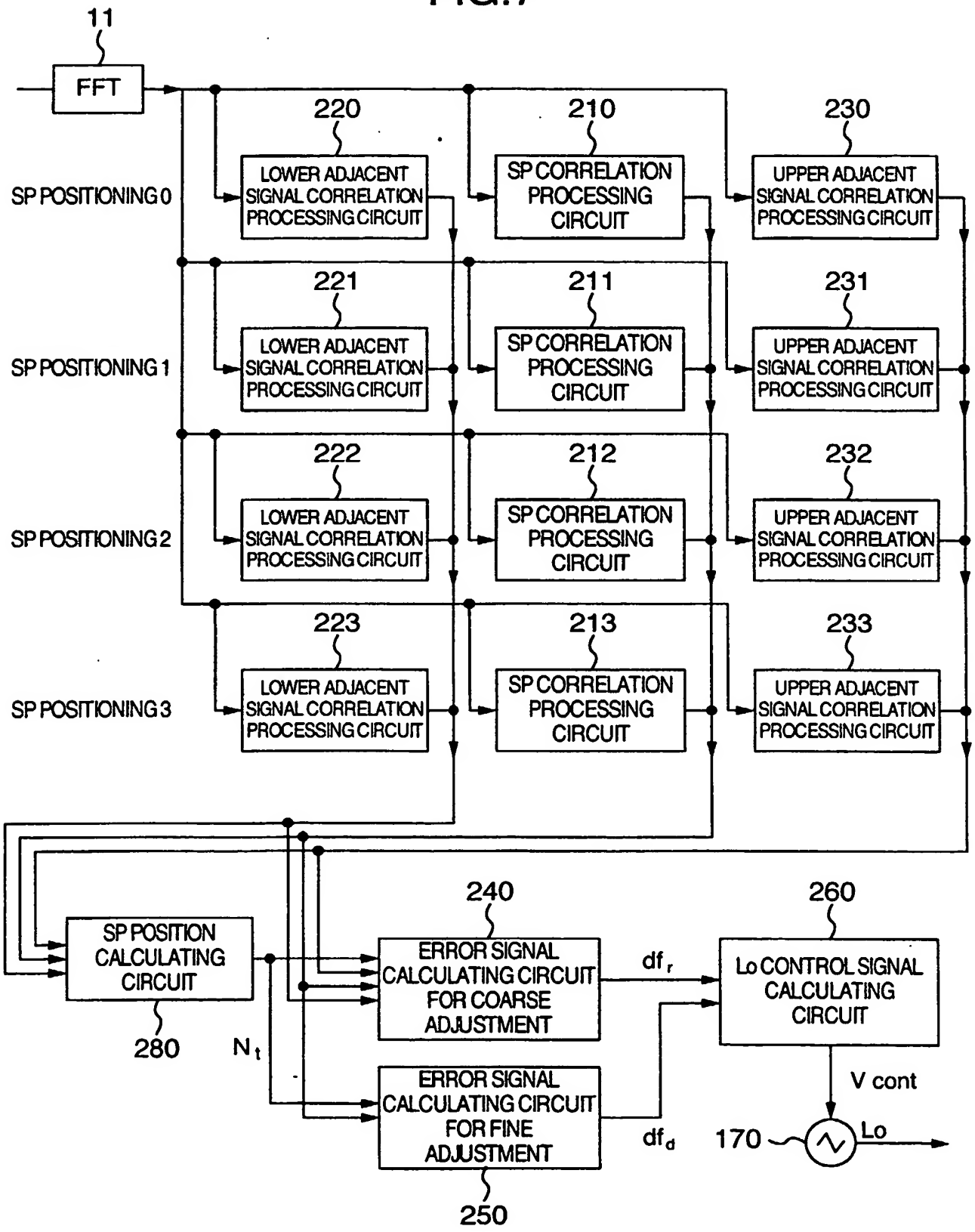

11
FFT
220
210
230
SP POSITIONING 0
LOWER ADJACENT SIGNAL CORRELATION PROCESSING CIRCUIT
SP CORRELATION PROCESSING CIRCUIT
UPPER ADJACENT SIGNAL CORRELATION PROCESSING CIRCUIT
221
211
231
SP POSITIONING 1
LOWER ADJACENT SIGNAL CORRELATION PROCESSING CIRCUIT
SP CORRELATION PROCESSING CIRCUIT
UPPER ADJACENT SIGNAL CORRELATION PROCESSING CIRCUIT
222
212
232
SP POSITIONING 2
LOWER ADJACENT SIGNAL CORRELATION PROCESSING CIRCUIT
SP CORRELATION PROCESSING CIRCUIT
UPPER ADJACENT SIGNAL CORRELATION PROCESSING CIRCUIT
223
213
233
SP POSITIONING 3
LOWER ADJACENT SIGNAL CORRELATION PROCESSING CIRCUIT
SP CORRELATION PROCESSING CIRCUIT
UPPER ADJACENT SIGNAL CORRELATION PROCESSING CIRCUIT
240
260
SP POSITION CALCULATING CIRCUIT
ERROR SIGNAL CALCULATING CIRCUIT FOR COARSE ADJUSTMENT
df r
Lo CONTROL SIGNAL CALCULATING CIRCUIT
280
N t
ERROR SIGNAL CALCULATING CIRCUIT FOR FINE ADJUSTMENT
V cont
df d
170
Lo
250

FIG.8

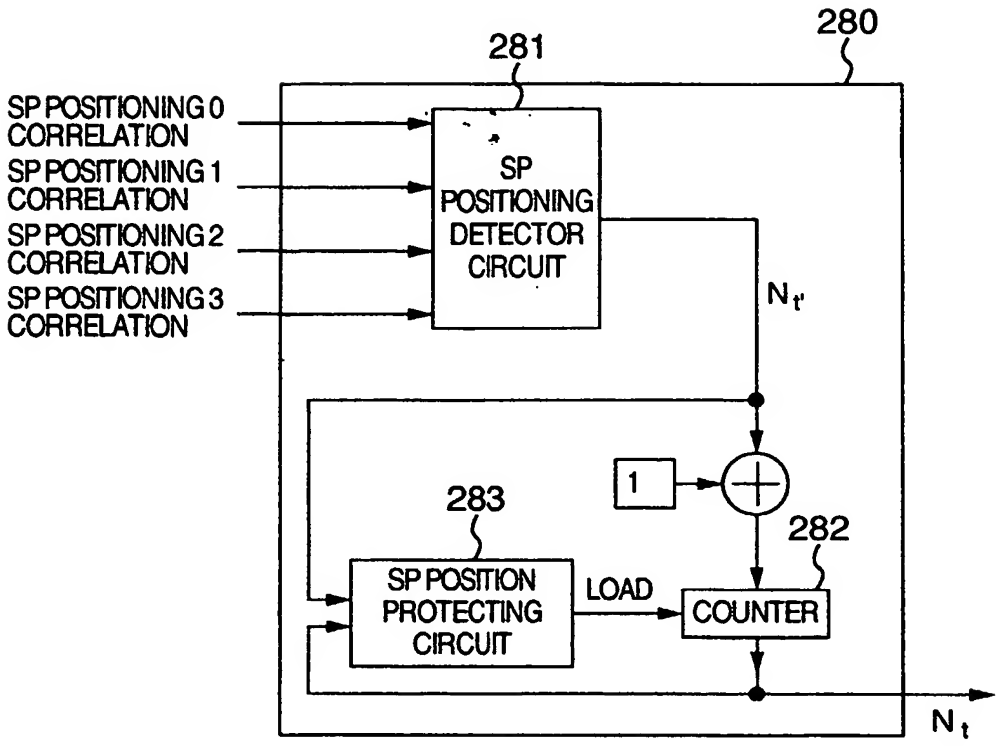

280
281
SP POSITIONING 0 CORRELATION
SP POSITIONING 1 CORRELATION
SP POSITIONING 2 CORRELATION
SP POSITIONING 3 CORRELATION
SP POSITIONING DETECTOR CIRCUIT
Nt'
1
283
282
SP POSITION PROTECTING CIRCUIT
LOAD
COUNTER
Nt

FIG.9

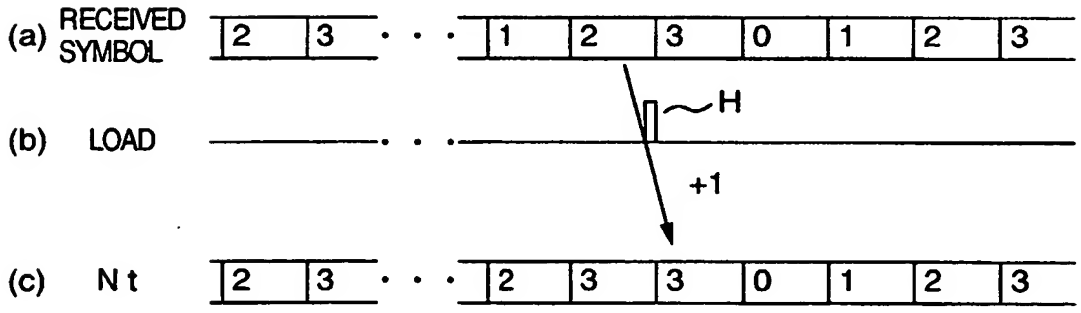

(a) RECEIVED SYMBOL
2 3 · · · 1 2 3 0 1 2 3
H
(b) LOAD
+1
(c) N t
2 3 · · · 2 3 3 0 1 2 3

FIG.10

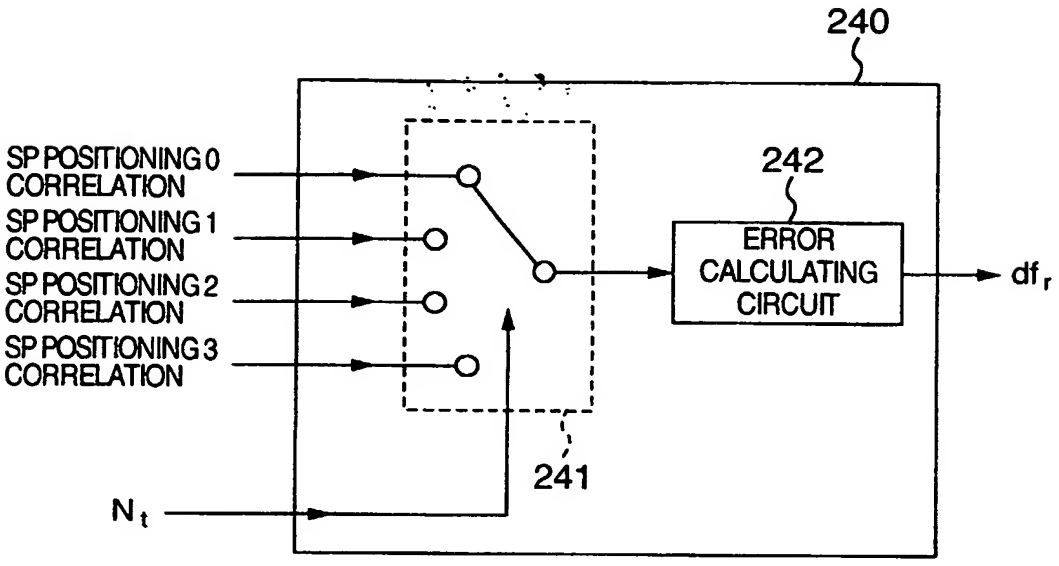

240
SP POSITIONING 0 CORRELATION
SP POSITIONING 1 CORRELATION
SP POSITIONING 2 CORRELATION
SP POSITIONING 3 CORRELATION
242
ERROR CALCULATING CIRCUIT
df_r
241
N_t

FIG.11

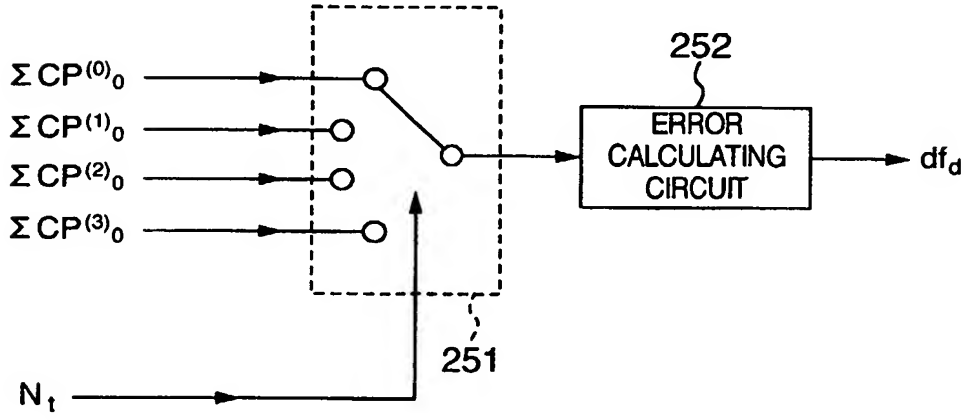

$\Sigma CP^{(0)}_0$
$\Sigma CP^{(1)}_0$
$\Sigma CP^{(2)}_0$
$\Sigma CP^{(3)}_0$
252
ERROR CALCULATING CIRCUIT
df_d
251
N_t

FIG.12

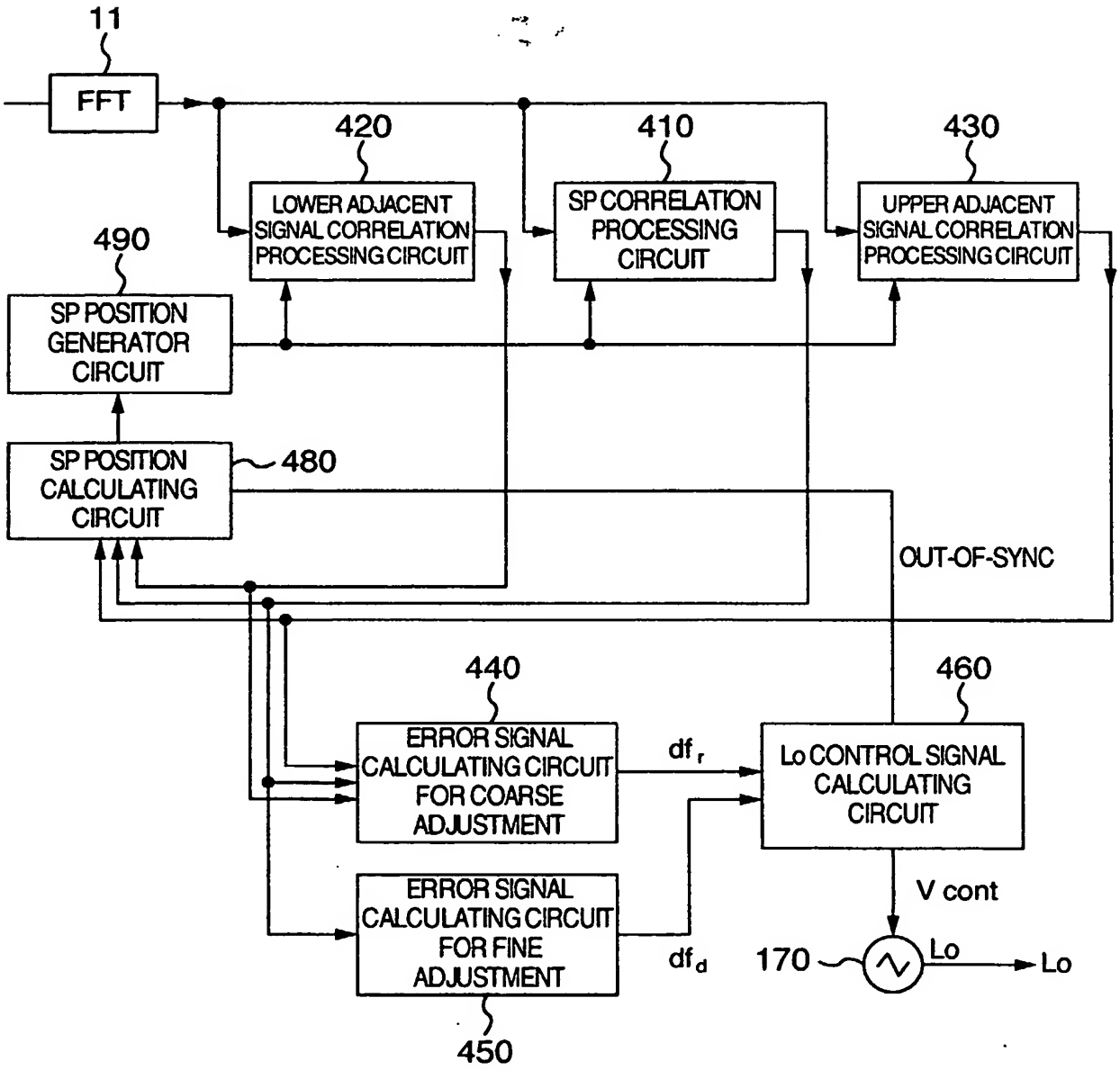

11
FFT
420
LOWER ADJACENT SIGNAL CORRELATION PROCESSING CIRCUIT
410
SP CORRELATION PROCESSING CIRCUIT
430
UPPER ADJACENT SIGNAL CORRELATION PROCESSING CIRCUIT
490
SP POSITION GENERATOR CIRCUIT
SP POSITION CALCULATING CIRCUIT
480
OUT-OF-SYNC
440
ERROR SIGNAL CALCULATING CIRCUIT FOR COARSE ADJUSTMENT
df r
460
Lo CONTROL SIGNAL CALCULATING CIRCUIT
V cont
ERROR SIGNAL CALCULATING CIRCUIT FOR FINE ADJUSTMENT
df d
170
Lo
Lo
450

FIG.13

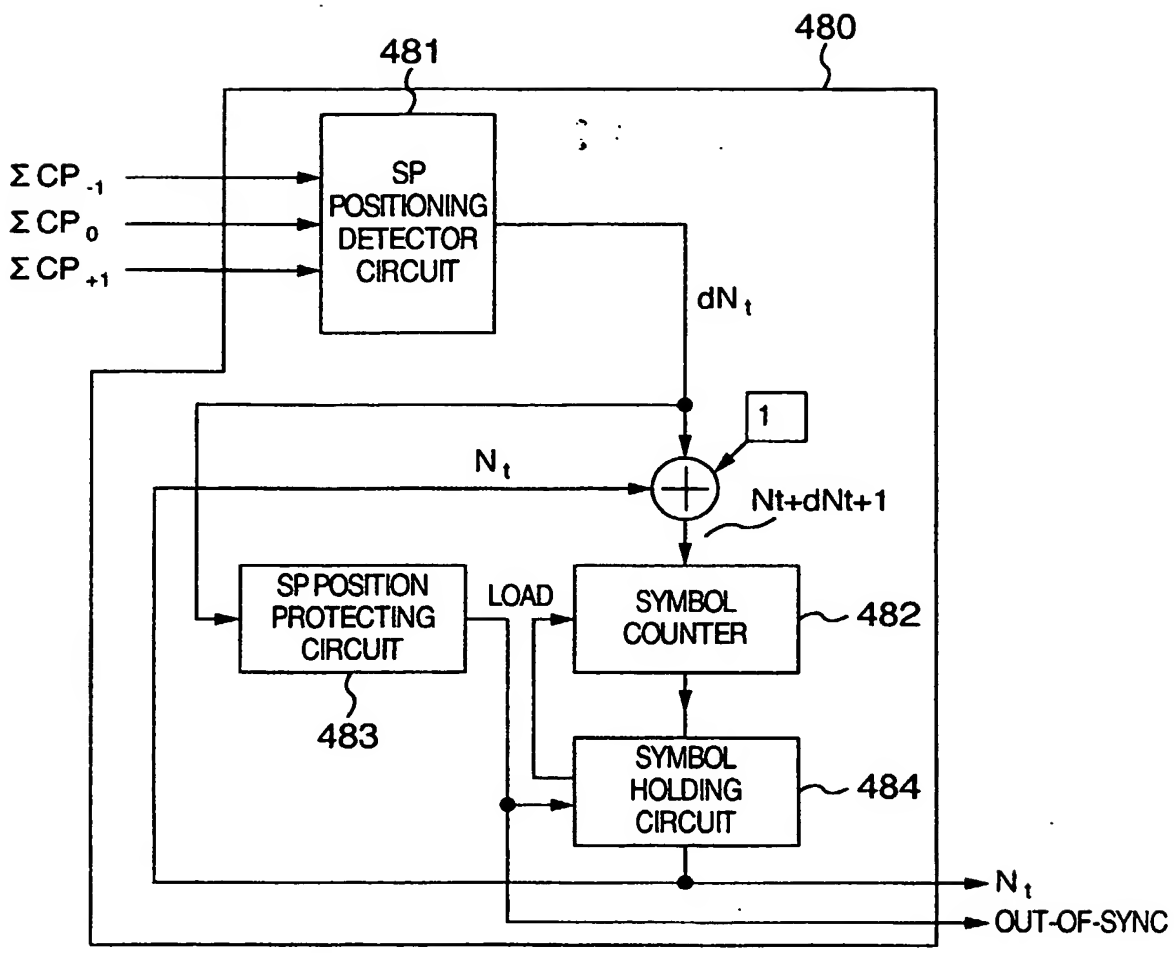

480
481
ΣCP-1
ΣCP0
ΣCP+1
SP POSITIONING DETECTOR CIRCUIT
dNt
1
Nt
Nt+dNt+1
SP POSITION PROTECTING CIRCUIT
LOAD
SYMBOL COUNTER
482
483
SYMBOL HOLDING CIRCUIT
484
Nt
OUT-OF-SYNC

FIG.14

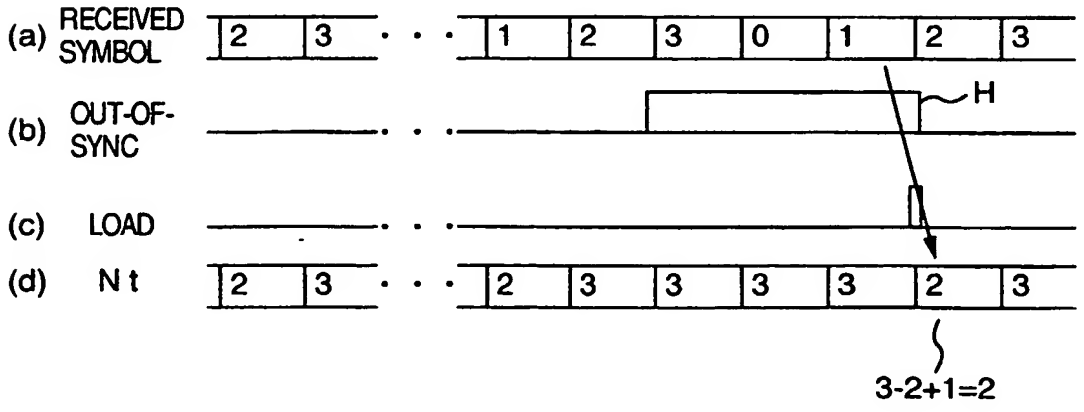

(a) RECEIVED SYMBOL
2 3 1 2 3 0 1 2 3
(b) OUT-OF-SYNC
H
(c) LOAD
(d) Nt
2 3 2 3 3 3 3 2 3
3-2+1=2

FIG.15

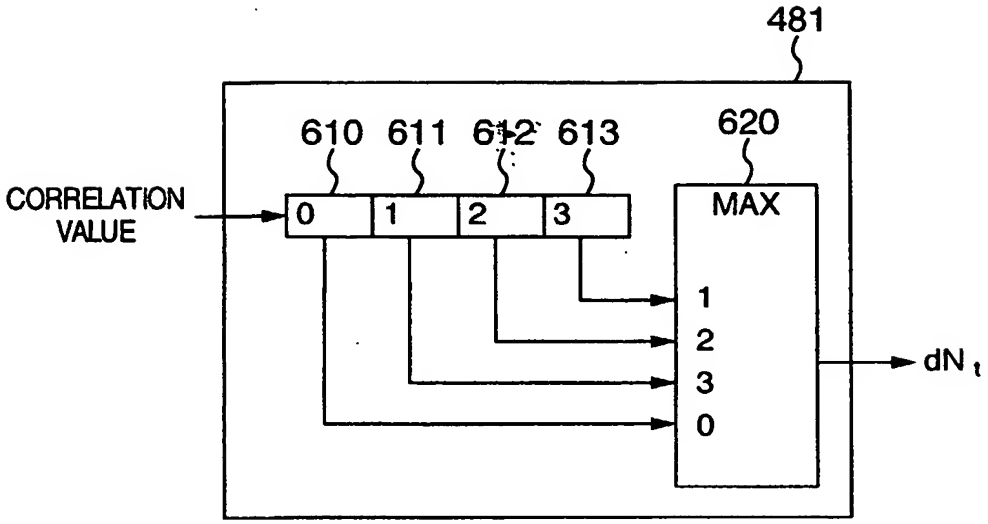

481
610
611
612
613
620
CORRELATION VALUE
0
1
2
3
MAX
1
2
3
0
dN t

FIG.16

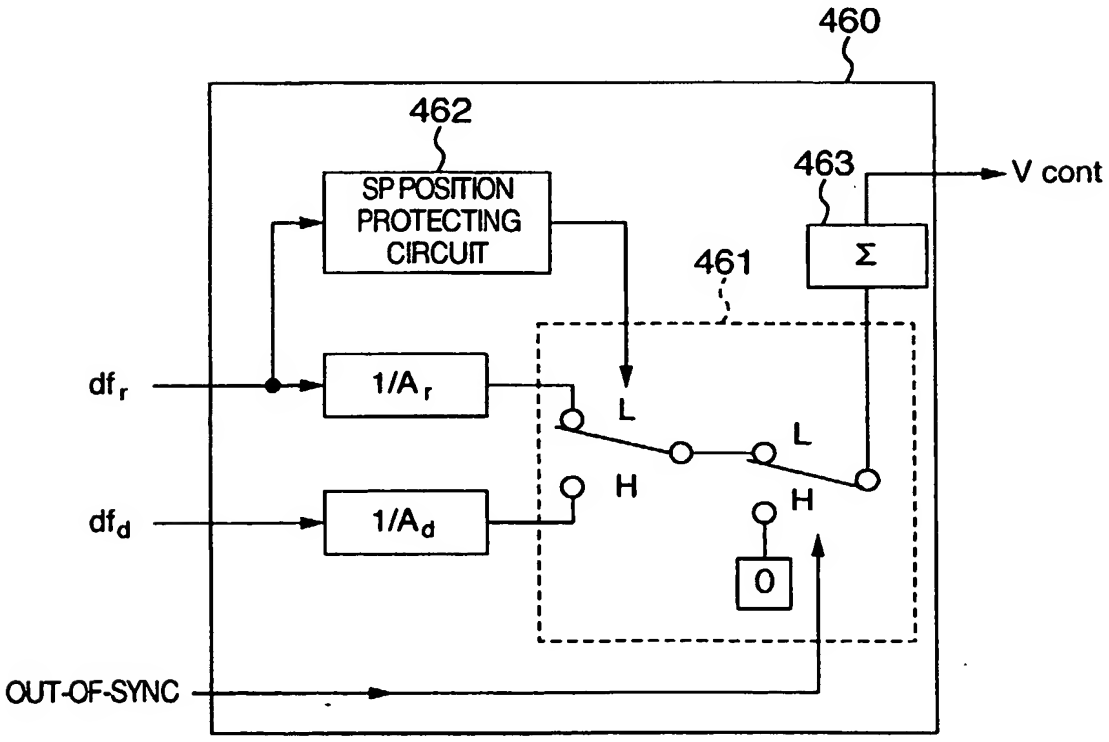

460
462
SP POSITION PROTECTING CIRCUIT
463
V cont
Σ
461
df r
1/A r
L
L
H
H
df d
1/A d
0
OUT-OF-SYNC

FIG.17

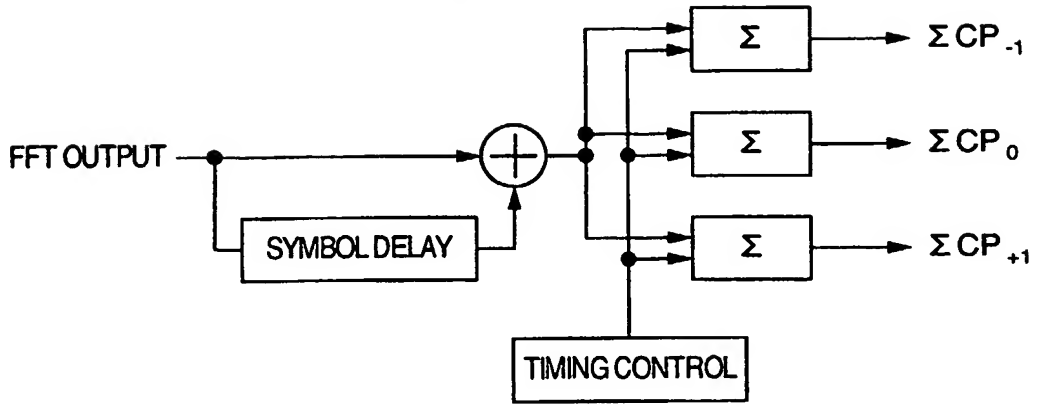

FFT OUTPUT
SYMBOL DELAY
TIMING CONTROL
Σ
Σ
Σ
Σ CP -1
Σ CP 0
Σ CP +1

FIG.18

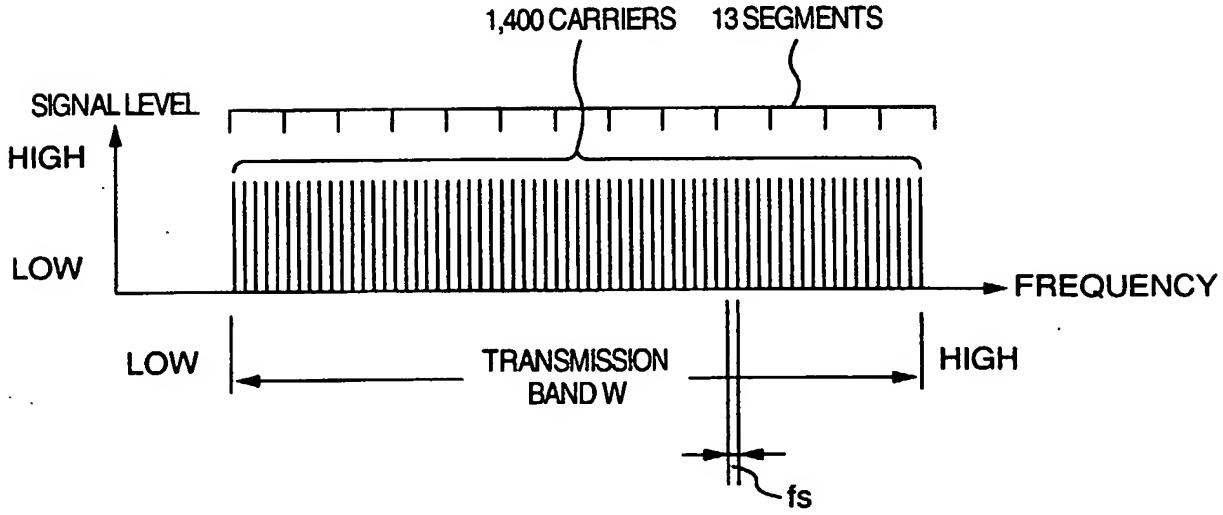

1,400 CARRIERS
13 SEGMENTS
SIGNAL LEVEL
HIGH
LOW
FREQUENCY
LOW
TRANSMISSION BAND W
HIGH
fs

FIG.19

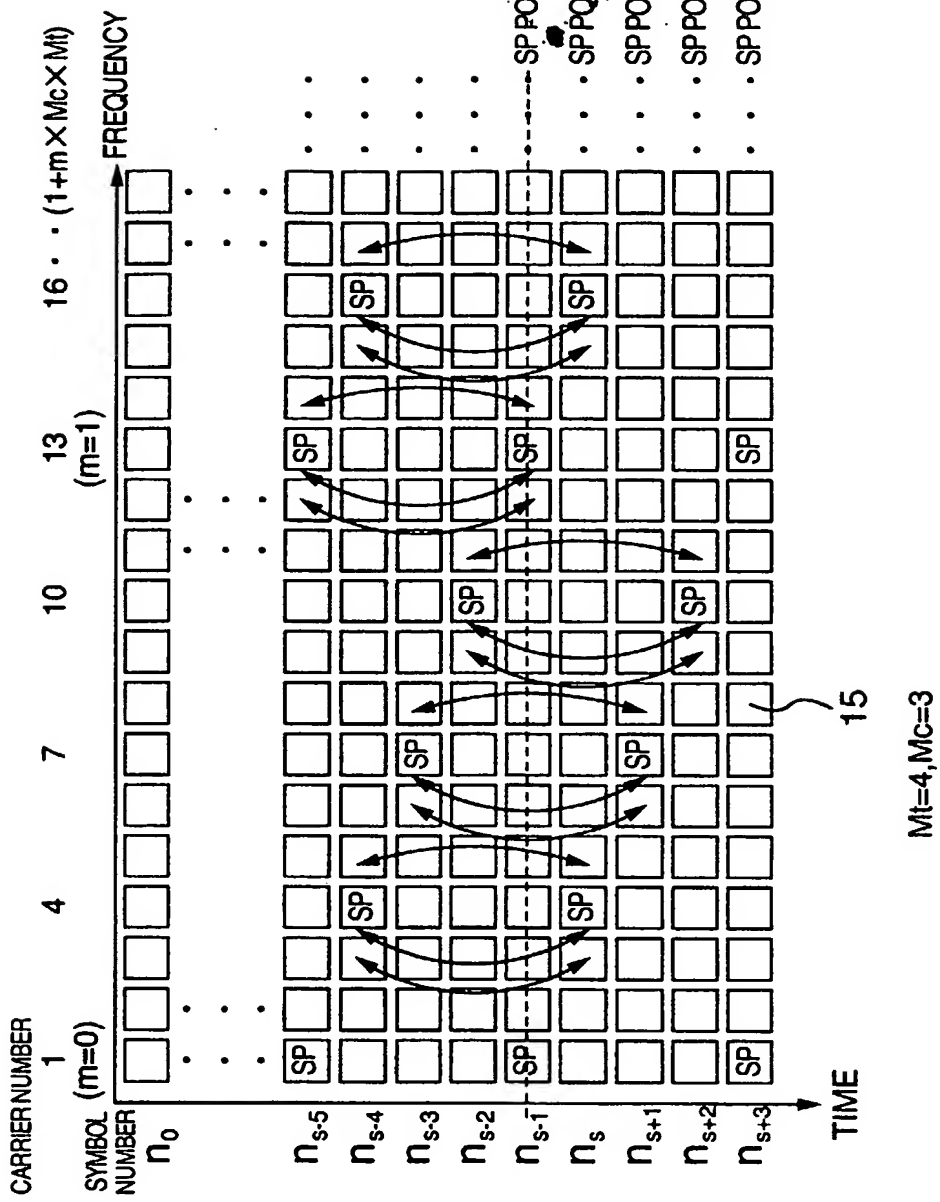

CARRIER NUMBER
1
4
7
10
13 (m=1)
16 · · · (1+m×Mc×Mt)
FREQUENCY
SYMBOL NUMBER
(m=0)
n_0
n_{s-5}
n_{s-4}
n_{s-3}
n_{s-2}
n_{s-1}
n_s
n_{s+1}
n_{s+2}
n_{s+3}
SP
SP POSITIONING 0
SP POSITIONING 1
SP POSITIONING 2
SP POSITIONING 3
SP POSITIONING 0
15
TIME
Mt=4,Mc=3

FIG.20

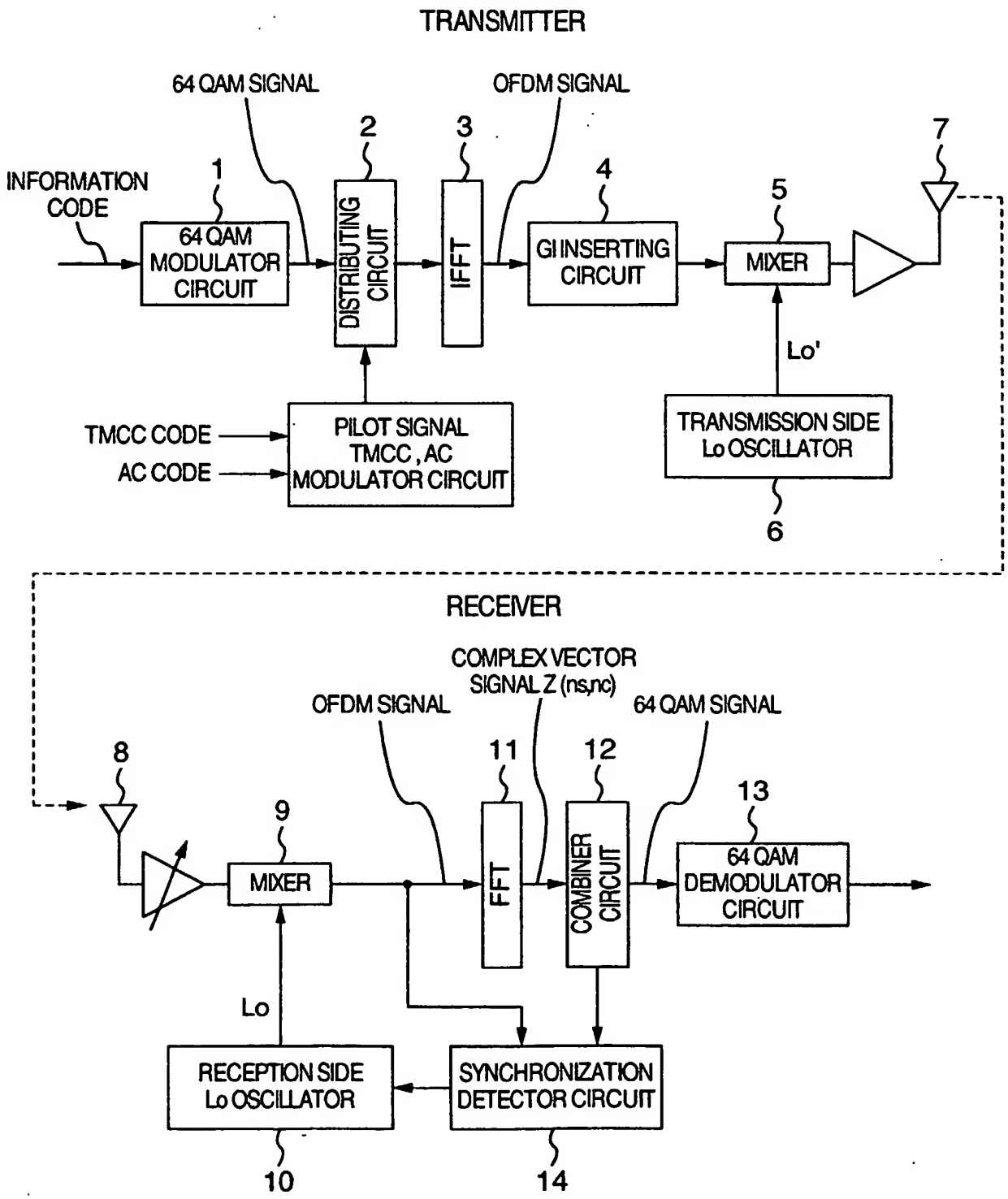

TRANSMITTER
64 QAM SIGNAL
OFDM SIGNAL
INFORMATION CODE
1
2
3
4
5
7
64 QAM MODULATOR CIRCUIT
DISTRIBUTING CIRCUIT
IFFT
GI INSERTING CIRCUIT
MIXER
Lo'
TMCC CODE
AC CODE
PILOT SIGNAL TMCC, AC MODULATOR CIRCUIT
TRANSMISSION SIDE Lo OSCILLATOR
6
RECEIVER
COMPLEX VECTOR SIGNAL Z (ns,nc)
OFDM SIGNAL
64 QAM SIGNAL
8
9
11
12
13
MIXER
FFT
COMBINER CIRCUIT
64 QAM DEMODULATOR CIRCUIT
Lo
RECEPTION SIDE Lo OSCILLATOR
SYNCHRONIZATION DETECTOR CIRCUIT
10
14

FIG.21

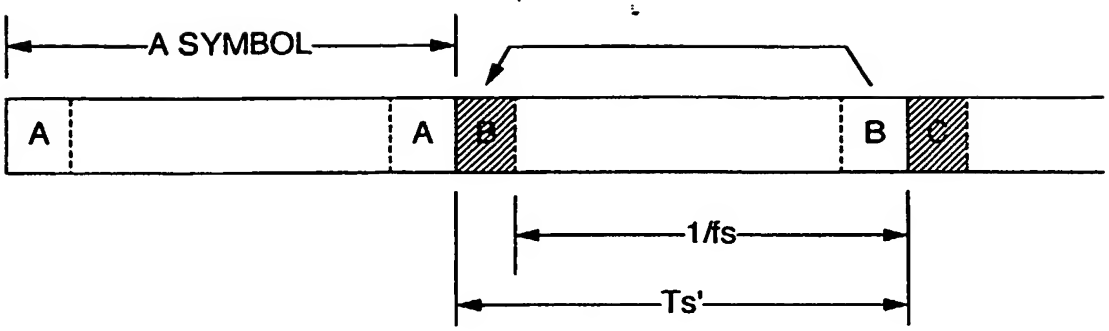


FIG.22

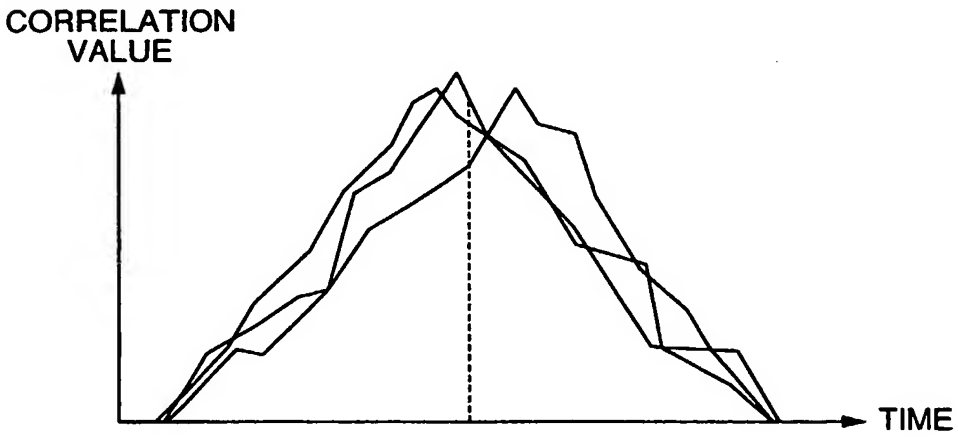
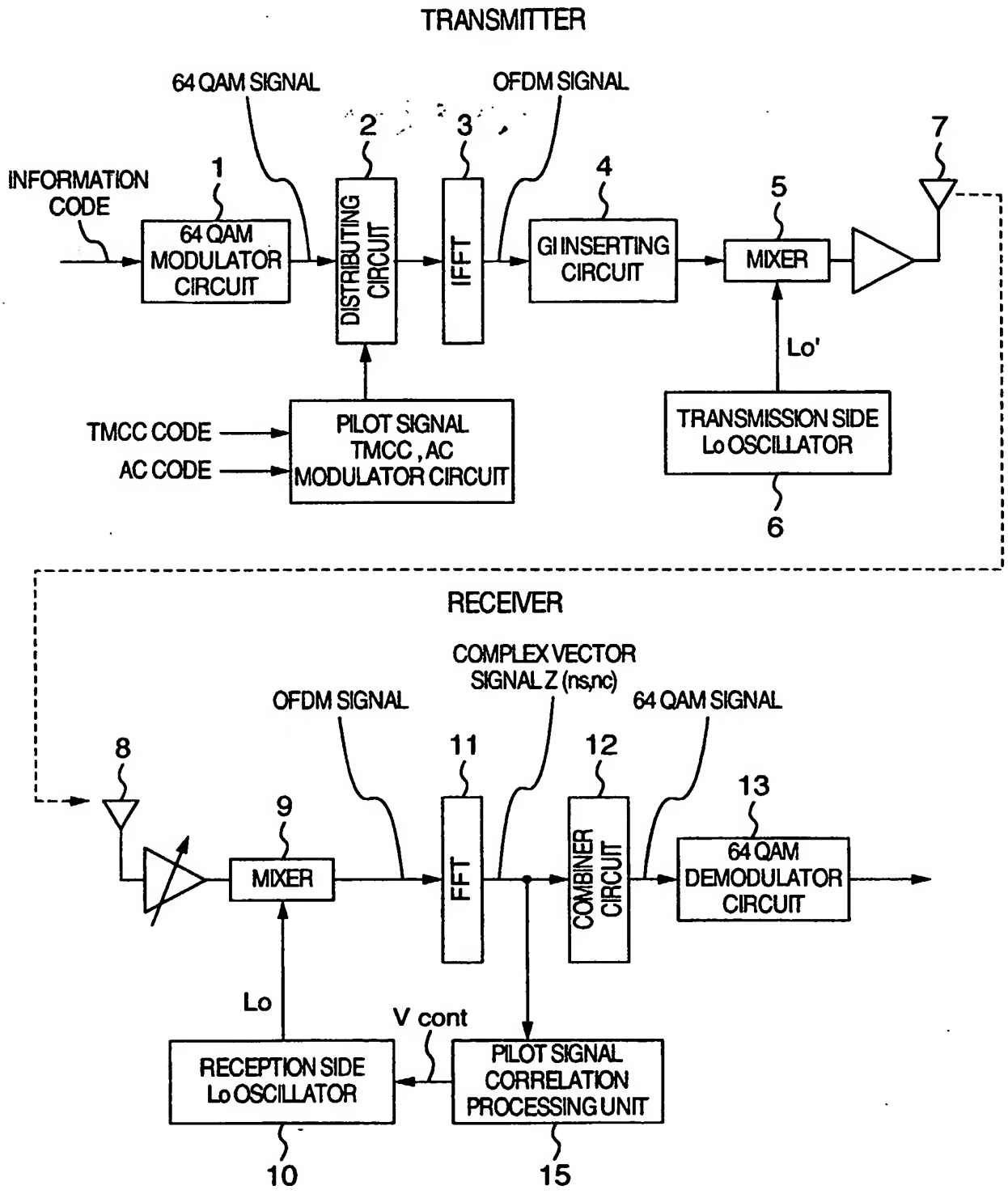


FIG.23


TRANSMITTER
64 QAM SIGNAL
OFDM SIGNAL
INFORMATION CODE
1
2
3
4
5
7
64 QAM MODULATOR CIRCUIT
DISTRIBUTING CIRCUIT
IFFT
GI INSERTING CIRCUIT
MIXER
Lo'
TMCC CODE
AC CODE
PILOT SIGNAL TMCC , AC MODULATOR CIRCUIT
TRANSMISSION SIDE Lo OSCILLATOR
6
RECEIVER
COMPLEX VECTOR SIGNAL Z (ns,nc)
OFDM SIGNAL
64 QAM SIGNAL
8
11
12
13
9
MIXER
FFT
COMBINER CIRCUIT
64 QAM DEMODULATOR CIRCUIT
Lo
V cont
RECEPTION SIDE Lo OSCILLATOR
PILOT SIGNAL CORRELATION PROCESSING UNIT
10
15

The present invention relates to a receiving apparatus for use with a signal transmission apparatus which employs as a transmission scheme the orthogonal frequency division multiplexing (hereinafter abbreviated as the "OFDM") for transmitting information codes with a plurality of carriers orthogonal to one another. Particularly, the receiving apparatus performs a novel method of synchronously reproducing a locally oscillated frequency (Lo frequency) of the signal transmission apparatus of OFDM which modulates the plurality of carriers of the OFDM using a modulation scheme for which synchronous detection is used (hereinafter called the "synchronous modulation scheme").

In the field of radio devices, the OFDM has been recently in the limelight as a modulation scheme immune to multipath fading. A large number of applied studies on the OFDM are now under progress in the fields of next-generation television broadcasting, FPU (Field Pick-up Unit), radio LAN and so on in many countries including European countries and Japan. Among these applied studies, the trends of developments in OFDM-based UHF-band terrestrial digital broadcasting and associated schemes are disclosed in detail in "The

Journal of the Institute of Image Information and Television Engineers," Vol. 52, No.11, pp. 1539-1545 and pp. 1658-1665 (1998).

As an example of the prior art, the UHF-band terrestrial digital broadcasting system in Japan will be described below in terms of system configuration. It should be noted however that this scheme involves an extremely complicated configuration, so that the following description will be made on the system which is simplified to such an extent that is required for understanding the present invention.

Fig. 18 is a diagram for explaining the structure of carriers in this broadcasting system. The OFDM digitally modulates several hundreds or more of carriers spaced from each other by a constant interval of frequency fs at a symbol frequency fs' (=1/Ts') for transmission, respectively, where Ts' represents a symbol period of a digital signal.

In the terrestrial digital broadcasting system in Japan, the system uses a total of approximately 1,400 carriers which are divided into 13 segments. As signals to be transmitted, information codes of up to three channels (three layers) can be simultaneously transmitted, and the number of segments and a modulation scheme used in each layer can be freely selected from several modes as shown in the above-mentioned document. Within such selectable modes, a mode which modulates carriers of all segments

in accordance with the same synchronous modulation scheme, such as 64 Quadrature Amplitude Modulation (64QAM), can be applied as it is to other transmitters such as FPU (Field Pick-up Unit).

Here, as a prior art example of OFDM-based transmission apparatus which modulates in accordance with a synchronous modulation scheme, a specific example in which carriers of all segments are modulated in accordance with the same 64QAM scheme to transmit information codes on one layer will be described in greater detail.

Fig. 19 is a diagram for explaining in greater detail the carrier structure of segments which are modulated in accordance with the synchronous modulation scheme. In this event, in a mode which uses all segments for transmission of information codes on one layer, it may be thought that a similar structure is repeated over the associated band.

Referring specifically to Fig. 19, the horizontal direction represents the frequency; the vertical direction represents the lapse of time; and each of squares "□" arrayed in the horizontal and vertical directions represents one carrier. Thus, one row of squares "□" arranged in the horizontal direction within the entire frequency band represents one symbol which forms part of an OFDM signal.

Further, a square mark "□" with "SP" denoted therein represents the position of a pilot signal which

is used for reproducing a reference signal during demodulation, while a square mark "□" without any notation therein represents the position of a signal modulated in accordance with the 64QAM scheme. As can be seen in Fig. 19, since the pilot signals are scattered in the frequency direction as well as in the time direction, they are designated as "SP" (Scattered Pilot).

It should be noted however that Fig. 19 merely indicates the positioning of the pilot signals SP's in a schematic form and omits a TMCC (Transmission and Multiplexing Configuration Control) carrier and an auxiliary information AC (Auxiliary Channel) carrier which should be essentially positioned therein for transmitting control signals. In the actual terrestrial digital broadcasting system, a plurality of consecutive carriers in the time direction, which have been modulated in accordance with Differential Binary Phase Shift Keying (DBPSK) with special data such as TMCC and AC as mentioned, are randomly inserted within the carrier structure of Fig. 19 for transmission.

Fig. 20 illustrates in block diagram form the basic structure of an OFDM-based transmission apparatus. A transmitter illustrated on the upper side comprises a 64QAM modulator circuit 1 for modulating an information code to be transmitted to a complex vector signal of 64QAM scheme (hereinafter denoted the "64QAM signal").

The 64QAM signal resulting from the modulation is assinged to respective carriers in a distributing circuit 2. After a pilot (SP) signal, a TMCC code, an AC code, and so on are inserted simultaneously into the 64QAM signal in the distributing circuit 2, the resulting 64QAM signal is inverse discrete fast Fourier transformed (IFFT) in an IFFT circuit 3. This transform causes the 64QAM signal to be transformed into a baseband OFDM signal, multiplexed in accordance with the OFDM, which is comprised of 1,400 carriers that have a symbol period equal to a time interval Ts' and are spaced by a frequency interval fs from each other, and orthogonal to one another.

Subsequently, a guard interval inserting circuit 4 adds a guard interval to the OFDM signal by copying an end portion of each symbol in the OFDM signal and appending the copied portion to the head of the symbol indicated by hatchings, as illustrated in Fig. 21. This guard interval is inserted to increase the immunity to multipath fading. However, since this aspect is not related directly to the present invention, detailed description thereon is omitted.

The OFDM signal with the guard interval added thereto is further inputted to a mixer 5 which frequency converts the OFDM signal into a signal in a high frequency band by a high frequency transmission side local oscillating signal Lo' generated by a

transmission side Local (Lo) oscillator 6. Then, the resulting signal is amplified the power and transmitted from a transmission antenna 7.

On the other hand, in a receiver illustrated on the lower side of Fig. 20, a signal received by a reception antenna 8 is amplified, and then inputted to a mixer 9 which mixes the received signal with a reception side local oscillating signal Lo generated by a reception side local (Lo) oscillator 10 for frequency conversion, to reproduce a multiplexed baseband OFDM signal. The OFDM signal is further discrete fast Fourier transformed (FFT) in a FFT circuit 11, and separated into complex vector signals $Z(n_S, n_C)$ of the basebands of the respective carriers, where n_S represents a symbol number of the received signal ((s+1)th symbol), n_C represents a carrier number of a separated carrier (c-th carrier counted from the carrier at the end on the lower frequency side), and s and c are positive integers including zero, respectively.

The separated complex vector signals $Z(n_S, n_C)$ of the respective carriers are re-arranged in the original time order in a combiner circuit 12 in a process reverse to that in the distributing circuit 2, and consequently returned to a temporally consecutive 64QAM signal which is then demodulated by a 64QAM demodulator circuit 13 to information codes which are finally outputted.

Though omitted in the foregoing description on the circuit, the demodulation of a received signal involves, for driving the FFT circuit 11, leading a synchronization relationship among the frequency of a clock generated in the receiver; the symbol period; and the locally oscillated frequency (Lo frequency) for downconverting a carrier frequency to a baseband frequency into the same synchronization relationship among respective signals included in the received signal itself.

For this purpose, it is necessary to accurately detect shift amounts of the respective signals from them and correct the frequency shifts. Thus, the detection of a shift amount for each synchronization is a critical factor in the receiver. A synchronization detector circuit 14 is responsible for the detection of synchronization. Though the terrestrial digital broadcasting system does not particularly define the synchronization lead-in method, an example of synchronization lead-in method is disclosed in "The Journal of the Institute of Image Information and Television Engineers," Technical Reports Vol. 23, No. 28, pp. 25-30.

The disclosed method takes advantage of the fact that the amount of frequency shift from the locally oscillated frequency in units of the number of carrier rows has a highly random nature with respect to the positions of carriers which have been inserted for

transmitting TMCC, AC and SP, and finds correlation values for carrier positions between previously defined reference carrier positions and the positions of carriers for TMCC and so on resulting from a received and demodulated signal to detect the amount of frequency shift from the correlation value.

On the other hand, the amount of frequency shift, i.e., an error from the locally oscillated frequency smaller than a carrier interval is detected from the sum of phases for guard correlation vectors obtained by a calculation involved in a correlation of a guard interval signal with an original signal for copying (guard correlation) in Fig. 21.

Here, the former is denoted as "error detection for coarse adjustment" meaning detection of an error for coarse adjustment in units of the number of carrier rows, while the latter is denoted as "error detection for fine adjustment" meaning detection of an error for fine adjustment.

The conventional synchronization lead-in method requires a large number of special carriers which have highly randomized positions for the error detection for coarse adjustment. Therefore, if an attempt is made to apply the synchronization lead-in method in a transmission apparatus other than that intended for the terrestrial digital broadcasting system such as FPU, this results in a problem that the synchronization lead-in method can be restrictively

utilized only in those apparatus which are capable of transmitting and receiving a signal having a special carrier structure.

Also, in this conventional method, when the locally oscillated (Lo) frequency is shifted, for example, by a frequency equal to 1.6 carriers, a shift of the locally oscillated frequency in units of the number of rows cannot be detected unless the local oscillated frequency is once lead into the frequency which is shifted exactly by two carrier such that signals on carriers such as TMCC can be demodulated. The conventional method is therefore disadvantageous in that a long time is required for initial synchronization pull-in.

In addition, the foregoing conventional synchronization pull-in method uses the guard correlation vector which is calculated through the guard correlation for the error detection for fine adjustment. However, the guard correlation is intended to find a correlation of OFDM signals which commonly have waveforms near noise. Therefore, the waveform of the OFDM signal near noise reflects to the guard correlation vector, causing the same to be very noisy signal.

Fig. 22 is a schematic diagram showing a plurality of overlapped amplitude waveforms for guard correlation vectors when the guard interval length is equal to 64 clocks. As is apparent from the figure,

the guard correlation vectors actually exhibit low SN (CN) ratio.

On the other hand, noise introduced into a control signal for the Lo frequency appears as it is as fluctuations in the Lo frequency. The noise further introduces into a 64QAM demodulated signal, causing degraded noise performance of the demodulated signal. For this reason, a detection method which causes small noise is required for the error detection for fine adjustment which is operative at all times during demodulation of 64QAM.

For reducing noise in the guard correlation vector, the guard interval length must be made as long as possible. However, when an attempt is made to apply the conventional frequency pull-in method in a transmission apparatus other than that intended for the terrestrial digital broadcasting system such as FPU, a significant restriction is imposed on the guard interval length.

The present invention provides a receiving apparatus which employs a synchronization reproducing method that can implement the error detection for coarse adjustment without using a large number of special carriers having highly randomized positions. The present invention also provides a receiving apparatus which employs a synchronization reproducing

method that can implement the error detection for fine adjustment in a high SN ratio without any restriction on the guard interval length.

The present invention provides a signal transmission system of orthogonal frequency division multiplexing having a transmitting apparatus and a receiving apparatus to transmit OFDM signal, wherein the receiving apparatus comprises; an input portion having an antenna, a mixer and a local oscillator, for receiving the OFDM signal from the transmitting apparatus; a fast Fourier transforming circuit coupled with the input portion to convert the OFDM signal into base-band signals having a plurality of carriers with a symbol frequency and a predetermined symbol period, the carriers including pilot signals; a demodulation unit coupled with the fast Fourier transforming circuit, for decoding to be produced as information codes; and a pilot signal correlation processing unit coupled with the local oscillator and the fast Fourier transforming circuit, for calculating a correlation value relating to said pilot signal, and controlling a frequency of the local oscillator based on the result of calculation of the correlation value.

The present invention is directed to a receiving apparatus in a signal transmission system of orthogonal frequency division multiplexing type for transmitting information codes on a plurality of carriers orthogonal to one another and frequencies

different from one another. A signal received by the receiving apparatus of the present invention includes a plurality of carriers wherein the pilot signals (CP) are positioned consecutively in the time axis direction on carriers at predetermined frequencies, and the pilot signals are positioned at intervals of a predetermined number of carriers in the frequency axis direction of the respective symbols. The receiving apparatus has a local oscillator for generating a locally oscillated signal for frequency converting the received signal into a predetermined frequency, a pilot signal correlation processing circuit for calculating correlation values between the pilot signal inserted in a carrier of an n_S-th received symbol in the predetermined frequency and the pilot signal inserted in the same carrier position of an (n_S-1)-th symbol preceding to the n_S-th received signal signal and calculating a correlation value signal ΣCP_0 which is the sum of the correlation values, and control means for detecting a phase component of the correlation value signal as an error in frequency of the locally oscillated signal generated by the local oscillator to control a frequency of the locally oscillated signal based on the error.

Further, a signal received by the receiving apparatus of the present invention includes a plurality of carriers at different frequencies on which pilot signals are positioned. The pilot signals are

positioned on carriers at predetermined frequencies at intervals of a predetermined number Mt of symbols in the time axis direction, wherein positions of carriers assigned with the pilot signals are inserted with a shift of a predetermined number Mc of carriers in every symbol in a frequency direction, and the pilots are inserted at predetermined carrier intervals (McxMt) in the frequency direction on the rows of the respective carriers. The receiving apparatus of the present invention has a local oscillator for generating a locally oscillated signal for frequency converting the received signal, a pilot signal correlation processing circuit for calculating correlation values between the pilot signal inserted in a carrier of at an n_S-th received symbol in the frequency direction and the pilot signal positioned at the same carrier position of an (n_S-M_t)-th symbol located a predetermined number Mt of symbols in front of the n_S-th received signal and calculating a correlation value signal ΣSP_0 which is the sum of the correlation values, and control means for detecting a phase component of the correlation value signal of the sum as an error in frequency of the locally oscillated signal generated by the local oscillator to control a frequency of the locally oscillated signal based on the error.

The receiving apparatus of the present invention having the configuration described above calculates correlation values in complex vector

representation between a pilot signal of a currently received symbol and a pilot signal at the same carrier position in the preceding symbol for a symbol period, and determines a frequency error from a phase component of the sum of the correlation values. The calculation for deriving the correlation value means that calculation of a product of the pilot signal of the currently received symbol and the pilot signal at the same carrier position in the preceding symbol for all pilot signals within the symbol is made, and summing the products is made. As described later, the phase angle of the correlation value thus calculated accurately corresponds to the amount of error in the frequency of a locally oscillated signal on the reception side from a locally oscillated frequency on the transmission side in a high SN ratio. By controlling the locally oscillated frequency on the reception side based on the error determined in this way in a direction in which the error becomes smaller, it is possible to reduce a time required to lead the received signal into synchronization.

The OFDM employing a synchronous modulation scheme corresponding to synchronous detection generally uses a carrier structure in which pilot signals are inserted. The present invention uses the pilot signals for coarse error detection of the local (Lo) frequency as well as fine error detection of the Lo frequency. Therefore, the present invention does not require a

large number of special carriers having highly randomized positions as before.

As a result, advantageously, it is possible to freely set the carrier structure suitable for a particular application without paying attention to the positioning of special carriers or restriction on the number of carrier rows.

Also, since the error detection of the present invention does not rely on the guard interval, the carrier structure can be freely set without significant restriction on the guard interval length as well.

Further, the conventional error detection for coarse adjustment cannot detect a shift of the locally oscillated frequency in units of the number of carrier unless the local oscillated frequency is once led into the frequency which is shifted by an integer number of carrier rows such that signals on carriers such as TMCC can be demodulated. The conventional method is therefore disadvantageous in that a long time is required for initial synchronization pull-in.

In contrast, the present invention is capable of detecting a shift in the Lo frequency at any time irrespective of the amount of shift in the Lo frequency at that time. Advantageously, this results in a reduction in time required for the initial synchronization pull-in.

The conventional synchronization pull-in

processing uses a guard correlation vector, found by a guard correlation, for the error detection for fine adjustment. Since an OFDM signal is mixed with a large number of carriers at different frequencies, its temporal wavelength appears to be a waveform which resembles noise.

On the contrary, the present invention separates signals included in an OFDM signal one by one of carriers to extract pilot signals included in each signal for calculating correlation values. In other words, unlike the OFDM signal having a plurality of carriers mixed therein, each pilot signal of each carrier exhibits a high SN ratio identical to a signal on a carrier modulated in accordance with 64QAM. Therefore, correlation values can also be calculated in a higher SN ratio as compared with the guard correlation vector. Consequently, the error detection for fine adjustment can also be accomplished with less noise.

In this way, the present invention, when employed, can perform the error detection for coarse adjustment without using a large number of special carriers having highly randomized positions. In addition, the error detection for fine adjustment can be accomplished in a high SN ratio without any restriction on the guard interval length.

A preferred embodiment of the invention will now be described with reference to the accompanying drawings in which:

Fig. 1 is a block diagram illustrating the configuration of a first embodiment of an Lo frequency shift detector circuit according to the present invention;

Fig. 2 is a schematic diagram showing the structure of carriers used in the first embodiment of the present invention;

Fig. 3 is a diagram for explaining correlation processing in the first embodiment of the present invention;

Fig. 4 is a characteristic graph showing an error signal for fine frequency adjustment in the first embodiment of the present invention;

Fig. 5 is a characteristic graph showing an error signal for coarse frequency adjustment in the first embodiment of the present invention;

Fig. 6 is a block diagram illustrating an Lo control signal calculating circuit in the first embodiment of the present invention;

Fig. 7 is a block diagram illustrating the configuration of a second embodiment of the Lo frequency shift detector circuit according to the present invention;

Fig. 8 is a block diagram illustrating the circuit configuration of an SP positioning calculating

circuit in the second embodiment of the present invention;

Fig. 9 is a time chart for explaining the operation of SP positioning protection processing in the second embodiment of the present invention;

Fig. 10 is a block diagram illustrating the configuration of an error signal calculating circuit for coarse adjustment in the second embodiment of the present invention;

Fig. 11 is a block diagram illustrating the configuration of an error signal calculating circuit for fine adjustment in the second embodiment of the present invention;

Fig. 12 is a block diagram illustrating the configuration of a third embodiment of the Lo frequency shift detector circuit according to the present invention;

Fig. 13 is a block diagram illustrating an exemplary circuit configuration of an SP positioning calculating circuit in the third embodiment of the present invention;

Fig. 14 is a time chart for explaining the operation of SP positioning protection processing in the third embodiment of the present invention;

Fig. 15 is a block diagram illustrating the configuration of an SP positioning detector circuit in the third embodiment of the present invention;

Fig. 16 is a block diagram illustrating the

configuration of an Lo control signal calculating circuit in the third embodiment of the present invention;

Fig. 17 is a block diagram illustrating another circuit configuration of the correlation processing circuit in the first embodiment of the present invention;

Fig. 18 is a schematic diagram for explaining the structure of carriers in the terrestrial digital broadcasting system in Japan;

Fig. 19 is a detailed explanatory diagram of the structure of carriers in the terrestrial digital broadcasting system in Japan;

Fig. 20 is a block diagram illustrating the basic configuration of an OFDM-based transmission system;

Fig. 21 is a schematic diagram for explaining how a guard interval is added to a symbol;

Fig. 22 is a diagram for explaining waveforms of guard correlation vectors; and

Fig. 23 is a block diagram showing a whole structure of OFDM transmission system according to the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Fig. 1 illustrates a first embodiment of a circuit for detecting a shift in Lo frequency according to the present invention which will now be described

with reference to this figure. Fig. 23 shows a block diagram showing a structure of an OFDM signal transmission system according to one embodiment of the present invention. The blocks or elements of Fig. 23 and Fig. 20 attached with the same reference numerals are the same blocks or elements. Since the system configuration of Fig. 23 other than the pilot signal correlation processing unit 15 is basically same with that of Fig. 20, we will explain the embodiments of the invention in only different portions from the structure of Fig. 20. The pilot signal correlation processing unit 15 receives the complex vector signals from the FFT 11 and outputs control signal Vcont to the Lo oscillator 10. The detail internal circuit structure of pilot signal correlation processing unit 15 in the transmission system of Fig. 23 is shown in Fig. 1. Unlike the conventional carrier structure shown in Fig. 19, this embodiment employs a carrier structure in which pilot signals are consecutively inserted in the time-axis direction, as shown in Fig. 2. For clearly distinguishing the positions at which the pilot signals are inserted in the structure of Fig. 2 from the positions indicated by SP at which the pilot signals are sporadically inserted as shown in Fig. 19, the positions at which the pilot signals are inserted in Fig. 2 are indicated by a different reference letter CP (Continual Pilot) which emphasizes the continuity.

For the convenience of explanation, a method

of detecting an error for fine adjustment will be first explained, though a synchronization pull-in procedure is generally performed in the reverse order, i.e., first for coarse adjustment and then for fine adjustment.

A pilot signal (CP) correlation processing circuit 110 and an error signal calculating circuit 150 for fine adjustment in Fig. 1 are circuits which are associated with the error detection for fine adjustment.

In Fig. 1, an output signal of an FFT circuit 11, which has been expanded over signals on respective carriers, is inputted to the CP correlation processing circuit 110. The CP correlation processing circuit 110 calculates and outputs correlation values of a signal CP (n_S, 1+mxMc) of a currently received symbol n_S at a carrier at which CP is inserted (CP carrier) in Fig. 2 with a signal CP(n_S-1, 1+mxMc) at the same carrier position of the symbol (n_S-1) preceding to the currently received signal. More specifically, the CP correlation processing circuit 110 calculates a CP correlation value signal $\Sigma CP_0(n_S)$ in complex vector representation according to the following equation, and outputs the resulting correlation value signal $\Sigma CP_0(n_S)$:

$$\Sigma CP_0(n_S) = \Sigma_m\{CP(n_S, 1+mxMc) \times CP^*(n_S-1, 1+mxMc)\} \quad (1)$$

where Mc is a carrier interval at which the pilot

signals CP are inserted in a carrier direction; m, which is an integer 0, 1, ..., H-1, H, indicates the number of carrier rows including pilot signals within one symbol; and (1+mxMc) represents a carrier number at which a CP carrier is inserted. In the structure shown in Fig. 2, Mc=5 is employed. When the total number of carriers in one symbol is 1,400, H=1400/5. Also, CP*( ) represents a complex conjugate complex number of CP( ), and Σ_m represents the sum of calculation results $CP(n_S, 1+mxMc) \times CP^*(n_S-1, 1+mxmc)$ for m=0 to H-1. Correlation values of carriers in the positional relationship indicated by arrows in Fig. 2 are calculated within the same symbols, and the correlation value signal is derived from the equation (1).

The correlation value signal $\Sigma CP_0(n_S)$ outputted from the CP correlation processing circuit 110 is inputted to the error signal calculating circuit 150 for fine adjustment which calculates an error signal representative of the amount of shift in an Lo frequency. However, prior to describing the calculation of the error signal, the meaning of the foregoing equation (1) will be described in greater detail.

Generally, the phase of a complex vector signal $CP(n_S, 1+mxMc)$ largely varies from one carrier position to another due to influences such as multipath fading. However, the complex vector signal $CP(n_S, 1+mxMc)$ is substantially equal in phase to the same

signal CP(n_S-1, 1+mxMc) on the same carrier of the preceding symbol, so that the direction of the complex vector derived by the complex multiplication within the braces {} in the equation (1) is substantially oriented in the direction of the real axis (I-axis) in CP signals at whichever carrier positions. The amount of shift in a phase angle of a complex vector derived by the complex multiplication within the braces in the equation (1) from the I-axis direction represents the rotational speed of the phase of the CP signal within one symbol, and proportional to the amount of shift in Lo frequency.

Fig. 3 schematically illustrates the calculation of the equation (1). Each solid line arrow in Fig. 3 represents a complex vector derived by the complex multiplication within the braces in the equation (1). Also, a circle at the leading end of each arrow represents noise possessed by the complex vector. While the complex vectors largely vary one by one in direction due to noise, a resulting complex vector after addition has a phase angle which is substantially equal to an average value of phase angles of complex vectors derived by the complex multiplication within the braces in the equation (1), i.e., a phase angle which represents the amount of shift in Lo frequency. In this event, while the amplitude of the complex vector after the addition is increased by a factor of H which is the number of CP

carrier rows, a noise component is increased only by a factor of $\sqrt{H}$.

For this reason, the complex vector after the addition of all the vectors provides a signal which has a significantly high CN (carrier-to-noise) ratio. Even assuming that a received OFDM signal presents a CN ratio of 22 dB, which is an unusable noise level, due to a code error rate of 10^{-2} resulting from 64QAM, addition of, for example, 80 CP carriers results in the complex vector after the addition having the CN ratio equal to 38dB (22dB-3dB+19dB=38dB), where -3dB is the amount of increased noise due to the complex multiplication, and 19dB is the amount of reduced noise due to the addition (10xlog(80)).

This result shows that the noise component in the correlation value signal for the CP signal, calculated by the equation (1), can be substantially ignored.

Moreover, advantageously, this method can automatically reduce the influence of an unusually lowered level of some CP signal, if any, due to selective fading. In other words, since the equation (1) squares the amplitude of the CP signal by the complex multiplication, the amplitude of the signal after the complex multiplication of the CP signal, which has the level lowered due to the selective fading, is further reduced and therefore contributes hardly to the result of the addition in the equation

(1).

It is therefore possible to minimize the influence of the noise introduced in the CP signal at a lower level. Conversely, a CP signal which presents an increased level and a high CN ratio gives a significantly large contribution, and advantageously increases the CN ratio of the correlation value signal resulting from the addition.

Bearing the foregoing knowledge in mind, the method of detecting an error for fine adjustment will be described again. Referring back again to Fig. 1, a correlation value signal $\Sigma CP_0(n_S)$ in complex vector representation having a very high CN ratio, outputted from the CP correlation processing circuit 110 is inputted to the error signal calculating circuit 150 for fine adjustment which calculates and outputs an error signal df_d for use in fine adjustment of the Lo frequency.

As described above, the amount of shift $\theta\Sigma_{CP}$ in phase angle of the calculated correlation value signal $\Sigma CP_0(n_S)$ from the I-axis is proportional to the amount of shift in the Lo frequency. Therefore, the most exact method would involve directly calculating the phase angle of the correlation value signal $\Sigma CP_0(n_S)$, and outputting the phase angle as the error signal df_d for fine adjustment. Generally, however, a circuit for calculating a more accurate phase angle of a complex vector disadvantageously requires a larger

circuit scale. Therefore, the calculating circuit can be simplified by approximating the phase angle.

It should be noted that the error signal for controlling the Lo frequency need not be the value precisely proportional to the amount of shift in the Lo frequency. The error signal df_d can be used as a control signal as long as the value of the control signal matches the amount of shift in the Lo frequency in a direction of decreasing or increasing trend.

Next described is an exemplary method of calculating an error signal, which satisfies the foregoing condition and can be implemented by a circuit of a relatively small scale.

This calculating method takes advantage of the fact that the following approximate equation is satisfied in a range in which the phase angle $\theta\Sigma_{CP}$ (in radian) of the correlation value signal $\Sigma CP_0(n_s)$ is sufficiently small:

$$\theta\Sigma_{CP} \doteq Q\Sigma_{CP}/|I\Sigma_{CP}| \qquad (2)$$

where the imaginary part of the correlation value signal $\Sigma CP_0(n_s)$ is denoted by $Q\Sigma_{CP}$, and the real part of the same by $I\Sigma_{CP}$. It should be noted however that with this approximate equation, the value of the right side suddenly increases as $\theta\Sigma_{CP}$ exceeds 45 degrees, and diverges to infinity at 90 degrees as indicated by a broken line curve in Fig. 4. Therefore, this approximate equation cannot be actually used near 90 degrees. Also, the above equation (2) alone is not

capable of detecting a large shift in the Lo frequency such as that resulting in a phase error of 90 degrees or more.

To overcome such inconvenience, the approximate equation (2) is modified to the following inequality.

Specifically, first, the value of $|Q\Sigma_{CP}|/|I\Sigma_{CP}|$ is previously calculated. Here, this value is denoted by $absq\Sigma_{CP}$.

When $0 \leq absq\Sigma_{CP} < 1$:

$df_d = sing(Q\Sigma_{CP}) \cdot absq\Sigma_{CP}$

when $1 \leq absq\Sigma_{CP}$:

$df_d = sing(Q\Sigma_{CP}) \cdot 1$

when $I\Sigma_{CP} \leq 0$

$df_d = sing(Q\Sigma_{CP}) \cdot 1$ (3)

where $sing(Q\Sigma_{CP})$ represents the polarity of $Q\Sigma_{CP}$.

The value of the approximate error signal df_d may be represented by a bold solid line curve shown in Fig. 4. Here, the amount of shift in the Lo frequency is generally several degrees or less when the synchronization is pulled in. Therefore, the approximate error signal df_d calculated by the foregoing inequality presents a fairly good approximation, and matches the value of the phase angle $\theta\Sigma_{CP}$ in radian.

It is therefore possible to readily set up a gain of a loop for controlling the Lo frequency and design a stable phase-lock loop system.

On the other hand, when $\theta\Sigma_{CP}$ shifts by 45 degrees or more, particularly by 90 degrees or more, the approximate error signal df_d presents a small value as compared with a value in radian which corresponds to the angle. For this reason, if a loop gain is adjusted to be optimal in a normal pull-in state, a pull-in time constant disadvantageously becomes larger at this time.

However, once the synchronization is pulled in, such a large frequency shift rarely occurs. Moreover, even if the phase angle shifts over 45 degrees or more, there is no doubt that the approximate error signal df_d can pull into the synchronization for certain.

While flexion points of the df_d curve in Fig. 4 are chosen at points at which $absq\Sigma_{CP}=1$ stands $(Q\Sigma_{CP}/|I\Sigma_{CP}|=1, -1)$, arbitrary points may be chosen therefor. However, for the sake of fabricating the circuit, it is advantageous to chose a value which is a power of two such as $absq\Sigma_{CP}=2$.

In this way, with the employment of the CP correlation processing circuit 110 and the error signal calculating circuit 150 for fine adjustment, highly accurate error detection can be implemented for fine adjustment using a correlation value which has an SN or CN ratio sufficiently higher than the guard correlation, without depending on the length of the guard interval.

Though the order is reversed, next described

is a method of detecting an error for coarse adjustment in the circuit of Fig. 1. In Fig. 1, the detection of an error amount for coarse adjustment is made using correlation value signals $\Sigma CP_{-1}(n_S)$, $\Sigma CP_{+1}(n_S)$ outputted from a lower adjacent signal correlation processing circuit 120 and an upper adjacent signal correlation processing circuit 130, respectively, in addition to the correlation value signal $\Sigma CP_0(n_S)$ in complex vector representation outputted from the CP correlation processing circuit 110.

Within these circuits, the lower adjacent signal correlation processing circuit 120 is supplied with the output signal of the FFT circuit 11 as is the case with the CP correlation processing circuit 110, and performs the same calculation as the CP correlation processing circuit 110. However, rather than calculating a correlation value for a CP carrier, the lower adjacent signal correlation processing circuit 120 calculates a correlation value for a carrier at a lower frequency which is immediately adjacent to the CP carrier on the lower side.

More specifically, the lower adjacent signal correlation processing circuit 120 calculates and outputs a correlation value signal $\Sigma CP_{-1}(n_S)$ which represents a correlation value between a signal $Z(n_S, (1+mxMc)-1)$ on a carrier adjacent to a CP carrier of a currently received symbol ns and a signal $Z(n_S-1, (1+mxMc)-1)$ at the same carrier position as a symbol

(n_S-1) preceding to the currently received symbol.

Completely in a similar manner, the upper adjacent signal correlation processing circuit 130 is supplied with the output signal of the FFT circuit 11 and performs the same calculation as the CP correlation processing circuit 110. However, conversely to the lower adjacent signal correlation processing circuit 120, the upper adjacent signal correlation processing circuit 130 calculates a correlation value for a carrier at a higher frequency which is immediately adjacent to the CP carrier on the higher side.

More specifically, the upper adjacent signal correlation processing circuit 130 calculates and outputs a correlation value signal $\Sigma CP_{+1}(n_S)$ which represents a correlation value between a signal $Z(n_S, (1+mxMc)+1)$ on a carrier adjacent to a CP carrier of a currently received symbol ns and a signal $Z(n_S-1, (1+mxMc)+1)$ at the same carrier position as the symbol (n_S-1) preceding to the currently received symbol.

The calculations performed in these circuits 120, 130 are completely similar to the calculation performed in the CP correlation processing circuit 110, wherein the correlation value signals $\Sigma CP_{-1}(n_S)$, $\Sigma CP_{+1}(n_S)$ have very high SN or CN ratios, similar to the correlation value signal $\Sigma CP_0(n_S)$. Actually, these three circuits can be implemented by the same circuit configuration except that carriers for use in the calculations are mutually shifted one by one.

The correlation value signals $\Sigma CP_0(n_S)$, $\Sigma CP_{-1}(n_S)$, $\Sigma CP_{+1}(n_S)$ outputted respectively from the CP correlation processing circuit 110, lower adjacent signal correlation processing circuit 120 and upper adjacent signal correlation processing circuit 130 are inputted to an error signal calculating circuit 140 for coarse adjustment which calculates and outputs an error signal df_r for coarse adjustment.

Prior to describing a calculation method performed in the error signal calculating circuit 140, brief description will be given on a relationship among the correlation value signals $\Sigma CP_0(n_S)$, $\Sigma CP_{-1}(n_S)$, $\Sigma CP_{+1}(n_S)$ when the Lo frequency is shifted.

Fig. 5 is an explanatory diagram showing that the current Lo frequency of a receiving apparatus is shifted by 0.7 carriers from the carrier frequency of a CP carrier of a received signal. The horizontal axis represents a frequency axis on which bold scales are marked at the positions of carriers. A carrier at a frequency position labeled "0" on the scale shows the position of a CP carrier indicated by a carrier counter of the receiving apparatus. A bold arrow represents a frequency position and magnitude of a CP carrier of the received signal.

As a received signal having the CP signal represented by the bold arrow is expanded on respective carriers in the FFT circuit 11, signal represented by thin arrows are generated as signals on the respective

carriers. Here, broken line curves represent curves of sine functions.

The correlation value signal in complex vector representation is calculated by the complex multiplication of the signals represented by the thin arrows in accordance with the equation (1), and adding H carriers to the resulting value, and has substantially the same relationship as that shown in Fig. 5.

The received signal also includes a signal on an adjacent carrier, represented by a bold broken line arrow, in addition to the CP signals. For this reason, a component of the signal represented by the bold broken line arrow is also introduced into each of carriers expanded in the FFT circuit 11, in addition to components of the CP signals represented by the thin arrows.

However, since the adjacent carrier represented by the bold broken line arrow is modulated in accordance with 64QAM and therefore is a carrier which has a randomly varying phase, the phase of the introduced component is distributed randomly as well. Therefore, complex vectors derived by the complex multiplication of the CP signals have the phases substantially identical in any CP's, and the magnitudes multiplied by H by the addition for calculating the correlation value, whereas the levels of components introduced from the adjacent carrier represented by the

bold broken line arrow cancel with each another and become smaller.

As a result, the correlation value signals $\Sigma CP_0(n_s)$, $\Sigma CP_{-1}(n_s)$, $\Sigma CP_{+1}(n_s)$ can be approximated by only components of the CP signals represented by the thin arrows.

Based on the foregoing fact, description will be made on a method of calculating the error signal df_r for coarse adjustment in the error signal calculating circuit 140 for coarse adjustment.

First, the three correlation value signals $\Sigma CP_0(n_s)$, $\Sigma CP_{-1}(n_s)$, $\Sigma CP_{+1}(n_s)$ inputted to the error signal calculating circuit 140 are compared in amplitude with one another to find the carrier with a maximum amplitude value.

Then, assume that df_r = 0 radian (no shift) when the correlation value signal $\Sigma CP_0(n_s)$ has a maximum amplitude value, wherein the carrier of a received signal matches in phase with the Lo signal; $df_r = -2\pi$ radian (-1 carrier shift) when the correlation value signal $\Sigma CP_{-1}(n_s)$ has a maximum amplitude value; and $df_r = +2\pi$ radian (+1 carrier shift) when the correlation value signal $\Sigma CP_{+1}(n_s)$ has a maximum amplitude value.

From this calculation, the amount of shift in the Lo frequency can be calculated in an accuracy of ± 0.5 carriers. For example, in Fig. 5, the largest amplitude value is presented by the correlation value

signal $\Sigma CP_{+1}(n_S)$ at the carrier position nearest from the frequency of the CP signal represented by the bold arrow. This results in $df_r = +2\pi$, thereby making it possible to detect that the Lo frequency is shifted by +1 carrier in an accuracy of ± 0.5 carriers.

This method, which uses the amplitudes of the correlation value signals, can further improve the detection accuracy. This method applies a method of calculating the amount of shift in Lo frequency using CW signals, described in JP-A-11-4209, to the three correlation value signals. One is picked up from this calculation method for showing an exemplary application to the present invention.

This calculation method takes advantage of the fact that the position of the CP signal represented by the bold arrow in Fig. 5 can be approximately expressed by the following equation:

$$df_r = 2\pi \times [(R_{max} \times n_{max} + R_{next} \times n_{next})/(R_{max} + R_{next})]$$

where n_{max} is a carrier number of a correlation value signal which gives the maximum amplitude value R_{max}; and n_{next} is a carrier number of a correlation value signal which gives the next largest amplitude value R_{next}. In the case of Fig. 5, $n_{max}=+1$, and $n_{next}=0$. However, for further reducing the amount of calculations, the error signal dr_f is calculated by an approximation expressed by the following inequality:

When $R_{max}/2>R_{next}$,

$dr_f = 2\pi \times n_{max} + 0$ (radian)

When $R_{max}/2 \leq R_{next}$,

$dr_f = 2\pi \times (n_{max} + n_{next})/2$ (radian)

From these calculations, a shift in the Lo frequency can be detected approximately in an accuracy of ± 1/4 carrier frequency. For calculating a more fractional value, a comparison may be made with a value divided by a smaller bit shift such as $R_{max}/4$, or an addition or subtraction value therebetween.

In this way, with the employment of the CP correlation processing circuit 110, lower adjacent signal correlation processing circuit 120, upper adjacent signal correlation processing circuit 130, and error signal calculating circuit 140 for coarse adjustment in Fig 1, the amount of shift in the Lo frequency can be detected in units of the number of carrier rows without using a large number of special carriers having highly randomized positions such as TMCC.

Moreover, the amount of shift in units of the number of carriers, and even the amount of shift smaller than the unit in some cases, can be immediately detected without involving useless manipulations, such as the Lo frequency is once pulled into a frequency shifted in units of an integer number of carriers, and then the amount of shift is detected in units of the number of carriers.

A Lo control signal calculating circuit 160

in Fig. 1 calculates a final control signal for the Lo frequency from the error signals df_r, df_d outputted from the error signal calculating circuit 140 for coarse adjustment and the error signal calculating circuit 150 for fine adjustment, respectively. Fig. 6 illustrates an exemplary configuration of the Lo control signal calculating circuit 160.

The error signal df_r for coarse adjustment is multiplied by $1/A_r$, and then inputted to an error signal selector circuit 161. Likewise, the error signal df_d for fine adjustment is multiplied by $1/A_d$, and then inputted to the error signal selector circuit 161. Here, A_r and A_d are a constant for defining a loop gain of a control system for coarse adjustment, and a constant for defining a loop gain of a control system for fine adjustment, respectively. When A_r and A_d are set to values which satisfy $A_r<A_d$, the time constant for coarse adjustment can be made smaller than the time constant for fine adjustment, thereby making it possible to reduce an initial synchronization pull-in time.

The error signal df_r for coarse adjustment is also inputted to a coarse adjustment protecting circuit 162 simultaneously. The coarse adjustment protecting circuit 162 outputs a coarse adjustment protection signal H which indicates that the Lo frequency has been pulled into synchronization in the coarse adjustment within the accuracy of the coarse adjustment when $df_r=0$

is satisfied. Conversely, the adjustment protecting circuit 162 outputs a coarse adjustment protection signal L which indicates that the state in which the coarse adjustment completes the pull-in must be released to again make a coarse adjustment when $df_r0 \neq 0$ is successively satisfied for a predetermined number of symbols.

The error signal selector circuit 161 further receives the error signals df_r/A_r, df_d/A_d, as well as the coarse adjustment protection signal, and selects one of the two error signals for outputting as an error signal dF for control. Specifically, the error signal selector circuit 161 selects df_r/A_r for outputting as dF, when it receives the coarse adjustment protection signal L which indicates that $df_r \neq 0$ is successively satisfied, in order to perform a coarse adjustment of the Lo frequency.

On the other hand, when receiving the coarse adjustment protection signal H which indicates $df_r=0$, the error signal selector circuit 161 selects df_d/A_d for outputting as dF, in order to perform a fine adjustment of the Lo frequency.

The error signal dF outputted from the error signal selector circuit 161 is inputted to an integrator circuit 163 which integrates the error signal dF to generate a control signal Vcont that is outputted as an output signal of the Lo control signal calculating circuit 160 in Fig. 1.

As the control signal Vcont is derived from the CP correlation value and outputted from the Lo control signal calculating circuit 160 as described above, a VCO 10 is applied with the control signal Vcont which has undergone a coarse correction for coarse adjustment when the Lo frequency experiences a large shift over an integer number of carriers, and is applied with the control signal which has undergone a fine correction for fine adjustment when the Lo frequency experiences a small shift over a fraction of a carrier. Thus, the Lo frequency can be rapidly and smoothly god into the synchronization to the carrier frequency of the received signal irrespective of the amount of shift in the Lo frequency.

The employment of this embodiment as described above enables the error detection both for coarse adjustment and for fine adjustment of the Lo frequency using the pilot signals which are generally inserted in information codes in the OFDM which employs the synchronous modulation scheme. It is therefore possible to freely set the carrier structure suitable for a particular application without paying attention to the positioning of special carriers or restriction on the number of carrier rows, as required before.

Similarly, the structure of a signal can be advantageously taken into consideration without paying attention to a large restriction on the guard interval length. Also advantageously, the Lo frequency can be

rapidly and smoothly synchronized to the carrier frequency of the received signal irrespective of the amount of shift in the Lo frequency, thereby reducing the pull-in time in the initial synchronization. Further advantageously, the error detection for fine adjustment can be accomplished in a high SN or CN ratio.

Next, a second embodiment is illustrated in Fig. 7 and described below as a circuit for detecting a shift in the Lo frequency according to the present invention.

The second embodiment applies the concept of the first embodiment to the carrier structure as shown in Fig. 19 in which the pilot signals SP's are dispersed thereover.

Specifically, instead of calculating the correlation value of CP signals, the second embodiment calculates a correlation value of the SP signals, and calculates an error signal using the phase angle and amplitude of the correlation value. It should be recalled that in the carrier structure shown in Fig. 19, the pilot signals SP's are intermittently inserted in the time direction. Together with this aspect, the second embodiment largely differs from the first embodiment in that the positions of carriers in which SP's are inserted differ from one symbol to another. Specifically, the positioning of SP's is repeated from SP Positioning 0 to SP Positioning 3, such as an SP

position of a symbol indicated by a one-dot chain line 15 in Fig. 19 (SP Positioning 0), an SP position of the next symbol (immediately below) (SP Positioning 1), ..., an SP position of the fourth symbol (SP Positioning 3).

To support this situation, a circuit illustrated in Fig. 7 comprises four pilot signal (SP) correlation processing circuits 210 - 213, the number of which is equal to the number of types of different SP positioning in the carrier direction shown in Fig. 19. The circuit of Fig. 1 is further modified such that a correlation value is calculated between a carrier of a currently received symbol ns and a carrier (n_S-Mt) which is located Mt symbols before the symbol ns, with Mt being equal to the interval between SP's in the time direction. Correlation values are calculated for associated carriers placed in the positional relationship indicated by arrows in Fig. 19 within the same symbol to derive the correlation value.

Specifically, the pilot signal correlation processing circuit 210 associated with SP Positioning 0 performs a calculation similar to the aforementioned equation (1) between a signal Z(n_S, 1+mxM_CxM_t) located at the SP position of the currently received symbol ns (SP positioning 0) and a signal (n_S-Mt, 1+mxM_CxM_t) located at the same carrier position of a symbol (n_S-Mt) located Mt symbols before the currently received symbol to calculate and output a correlation

value signal $\Sigma SP(0)_0(n_S)$ for SP Positioning 0. Here, Mc represents the number of intervals between carriers (pilot carriers) in which SP's are inserted in the time direction. In Fig. 19, Mt=4, and Mc=3. It should be noted that the foregoing description has referred to Z( ) rather than SP( ) because a (1+mxMcxMt)th carrier is not always SP depending on a symbol number of a currently received symbol.

Similarly, the pilot signal correlation processing circuit 211 associated with SP Positioning 1 calculates and outputs a correlation value signal $\Sigma SP(1)_0(n_S)$ for SP Positioning 1 between a signal $Z(n_S, (1+mxMcxMt)+Mc)$ located at the SP position of SP Positioning 1 and a signal $Z(n_S-Mt, (1+mxMcxMt)+Mc)$ located at the same carrier position of a symbol (n_S-Mt) located Mt symbols before the currently received symbol.

Subsequently, in a similar manner, the pilot signal correlation processing circuit 212 associated with SP Positioning 2 and the pilot signal correlation processing circuit 213 associated with SP Positioning 3 calculate and output a correlation value signal $\Sigma SP(2)_0(n_S)$ for SP Positioning 2, which is a correlation value signal for SP Positioning 2, and a correlation value signal $\Sigma SP(3)_0(n_S)$ for SP Positioning 3, which is a correlation value signal for SP Positioning 3, respectively.

Completely in a similar manner, the circuit

illustrated in Fig. 7 comprises four each of lower adjacent signal correlation processing circuits 220 - 223 and upper adjacent signal correlation circuits 230 - 233 corresponding to the pilot signal correlation processing circuits associated with SP Positioning 0 through SP Positioning 3.

Then, the lower adjacent signal correlation processing circuits 220 - 223 output four correlation value signals from a correlation value signal $\Sigma SP(0)_{-1}(n_S)$ for SP Positioning 0 to $\Sigma SP^{(3)}{}_{-1}(n_S)$ for SP Positioning 3. The upper adjacent signal correlation processing circuits 230 - 233 in turn output four correlation value signals from a correlation value signal $\Sigma SP^{(0)}{}_{+1}(n_S)$ for SP Positioning 0 to $\Sigma SP^{(3)}{}_{+1}(n_S)$ for SP Positioning 3.

Further, the circuit of Fig. 7 comprises an SP position calculating circuit 280 for supporting the carrier positions of SP's which differ from one symbol to another. The SP position calculating circuit 280 employs the aforementioned 12 (=4x3) correlation value signals inputted thereto to detect and output the SP positioning number of a currently received symbol.

Fig. 8 illustrates the internal circuit configuration of the SP position calculating circuit 280. An SP position detector circuit 281, which forms part of the SP position calculating circuit 280, is provided for detecting an SP positioning number N_t' of a currently received symbol, a symbol counter 282 is

provided for counting up the SP positioning number N_t, and an SP position protecting circuit 283 is provided for protecting the synchronization established for the cycle of SP positioning.

The 12 correlation signals inputted to the SP position calculating circuit 280 are delivered as they are to the SP position detector circuit 281. In Fig. 7, a flow of a set of three correlation value signals $\Sigma SP(n)_{-1}(n_s)$, $\Sigma SP(n)_0(n_s)$, $\Sigma SP(n)_{+1}(n_s)$ for SP Positioning n (=0-3) is represented by a single bold line. The SP position detector circuit 281 compares amplitude values of the 12 correlation value signals inputted thereto, and selects the SP positioning number which includes a correlation value signal with a maximum amplitude value. Then, the SP position detector circuit 281 outputs the selected SP positioning number N_t'.

In this event, the symbol counter 282 counts up and outputs the SP positioning number N_t. Then, the SP positioning number N_t is outputted to the outside from the SP position calculating circuit 280. Simultaneously, the SP positioning number N_t is inputted to the SP position protecting circuit 283 together with the SP positioning number N_t' detected by and outputted from the SP position detector circuit 281. Then, the PS position protecting circuit 283 determines whether or not the cycle of the SP positioning is out of synchronization.

A procedure of protection processing implemented by the SP position protecting circuit 283 will be described with reference to a timing diagram of Fig. 9. Fig. 9(a) shows a signal at a symbol period outputted from the FFT circuit 11 in Fig. 1. Each frame represents a symbol, and a number denoted within the frame indicates the SP positioning number N_t'. Fig. 9(c) shows the SP positioning number N_t outputted from the symbol counter 282.

The protection processing described below is performed during a period in which no effective signal exists within each symbol period, for example, during a period of guard interval. During a period in which an effective signal exists, the state of the symbol counter 282 is held. When the SP positioning number is correctly pulled into synchronization, the SP positioning number (a) of the output signal from the FFT circuit matches the SP positioning number (c) outputted from the symbol counter 282, as can be seen in a left-hand portion of Fig. 9. On the other hand, if the SP positioning number is out of synchronization, the SP positioning number of the output signal from the FFT circuit deviates from the SP positioning number outputted from the symbol counter 282, so that no match is found therebetween, as can be seen in a central portion of Fig. 9. The SP position protecting circuit 283 detects the out-of-synchronization of the SP positioning number by comparing the SP positioning

number N_t' detected by the SP position detector circuit 281 with the SP positioning number N_t counted by the symbol counter 282.

Specifically, when the input SP positioning number does not match, the number in Fig. 9(a) deviates from the number in Fig. 9(c), indicating that the SP position is out of synchronization. Thus, the SP position protecting circuit 283 detects that the synchronization of the SP position is out of synchronization when it determines that the relationship between the numbers in Figs. 9(a) and 9(c) satisfies $N_t \neq N_t'$ successively for a predetermined number of symbols. Then, the SP position protecting circuit 283 outputs an SP out-of-sync signal H which indicates that the SP position is out of synchronization. The waveform of the SP out-of-sync signal H is shown in Fig. 9(b).

Referring back to Fig. 8, the SP out-of-sync signal H outputted from the SP position protecting circuit 283 is inputted to a load trigger terminal of the symbol counter 282. In addition, the symbol counter 282 is also loaded with a value ($N_t'+1$) resulting from adding one to the SP positioning number N_t' outputted from the symbol counter 282 in preparation for the operation in the next symbol period. The extra "+1" added to the value is for counting up the counter. Alternatively, the symbol counter 282 may be counted up. Generally, the SP

positioning number synchronization lead-in can be completed in this single protection processing. However, if the SP position is still out of synchronization after the protection processing, the same operation is repeated until the synchronization is pulled in.

With the foregoing protection processing, the SP position calculating circuit 280 in Fig. 7 continues to output the SP positioning number N_t of a currently received signal during a normal period in which the SP positioning number is in synchronization. Conversely, when the SP positioning number is out of synchronization, the SP position calculating circuit 280 automatically detects the out-of-synchronization state, corrects the SP positioning number, and again establishes the synchronization for the SP positioning number.

In Fig. 7, a coarse adjustment is performed in the following procedure. First, an output signal of the FFT circuit 11 is inputted to all of the four pilot signal (SP) correlation processing circuits, four lower adjacent signal correlation processing circuits and four upper adjacent signal correlation processing circuits. Then, all of 12 (=4x3) correlation value signals outputted from these circuits are inputted to the SP position calculating circuit 280 and the error signal calculating circuit 240 for coarse adjustment, respectively.

The SP position calculating circuit 280 leads the SP positioning into synchronization through the aforementioned procedure, and calculates and outputs SP positioning number N_t (=0-3) for a currently received symbol.

The error signal calculating circuit 240 for coarse adjustment is supplied with the SP positioning number N_t outputted from the SP position calculating circuit 280 simultaneously with the 12 correlation value signals inputted thereto, and calculates and outputs an error signal df_r for coarse adjustment.

Fig. 10 illustrates an exemplary internal circuit configuration of the error signal calculating circuit 240 for coarse adjustment. In Fig. 10, a correlation value signal selector circuit 241 selects and outputs a set of three correlation value signals corresponding to the SP positioning number N_t of a currently received symbol from the 12 correlation value signals inputted thereto in accordance with the simultaneously inputted SP positioning number N_t. Likewise, in Fig. 10, a flow of the set of three correlation value signals associated with the respective SP positioning is represented by a single bold line.

An error calculating circuit 242 is supplied with the set of three correlation value signals selected by the correlation value signal selector circuit 241, which include a correlation value signal

outputted from an SP correlation processing circuit associated with SP positioning number N_t; a correlation value signal outputted from a lower adjacent signal correlation processing circuit associated with SP positioning number N_t; a correlation value signal outputted from an upper adjacent signal correlation processing circuit associated with SP positioning number N_t. Then, the error calculating circuit 242 performs a similar calculation to that performed by the error signal calculating circuit for coarse adjustment in the first embodiment to calculate and output an error signal df_r for coarse adjustment. The error calculating circuit 242 may be implemented by a circuit in the same configuration as the error signal calculating circuit 140 for coarse adjustment in the first embodiment.

In this way, even for the carrier structure shown in Fig. 19 in which the pilot signals SP are dispersed thereover, the amount of shift in the Lo frequency can be detected in units of the number of carriers without relying on a large number of special carriers such as the TMCC signal, which have highly randomized positions, in a manner similar to the first embodiment.

Moreover, the amount of shift in units of the number of carriers, and even the amount of shift smaller than the unit in some cases, can be immediately detected without involving useless operation, such as

the Lo frequency is once led into a frequency shifted in units of an integer number of carriers, and then the amount of shift is detected in units of the number of carriers. It is also possible to reproduce the synchronization for the cycle of SP positions in the carrier structure of Fig. 19.

Next, a fine adjustment in Fig. 7 is performed in the following procedure. First, all of four correlation value signals outputted from the four SP correlation processing circuits are inputted to the error signal calculating circuit 250 for fine adjustment. Simultaneously, an SP positioning number N_t outputted from the SP position calculating circuit 280 is inputted to the error signal calculating circuit 250 for fine adjustment.

Fig. 11 illustrates an exemplary internal circuit configuration of the error signal calculating circuit 250 for fine adjustment. The circuit configuration in Fig. 11 is identical to the circuit configuration in Fig. 10 except that inputted and selected correlation value signals are correlation value signals $\Sigma CP(n)_0(n_S)$ outputted from the respective SP correlation processing circuits associated with respective SP positioning.

Specifically, a correlation value signal selector circuit 251 selects a correlation value signal $\Sigma CP(Nt)_0(n_S)$ corresponding to SP positioning of a currently received symbol from four correlation value

signals $\Sigma CP(n)_0(n_s)$ inputted thereto in accordance with the simultaneously inputted SP positioning number N_t. Then, the correlation value signal $\Sigma SP(n)_0(n_s)$ associated with SP positioning number N_t, selected by the correlation value signal selector circuit 251, is inputted to the error calculating circuit 252.

Then, in a manner similar to the error signal calculating circuit for fine adjustment in the first embodiment, the error calculating circuit 252 calculates and outputs an error signal df_d for fine adjustment. The error calculating circuit 252 may be implemented by a circuit in the same configuration as the error signal calculating circuit 150 for fine adjustment in the first embodiment.

In this way, even for the carrier structure shown in Fig. 19 in which the pilot signals SP are dispersed over the carriers, highly accurate error detection for fine adjustment can be accomplished using a correlation value with an SN or CN ratio sufficiently higher than the guard correlation, without depending on the guard interval length.

Turning back to Fig. 7, an Lo control signal calculating circuit 260 is provided for calculating a final control signal Vcont for the Lo frequency from the error signals df_r, df_d respectively outputted from the error signal calculating circuit 240 for coarse adjustment and the error signal calculating circuit 250 for fine adjustment. The Lo control signal calculating

circuit 260 calculates and outputs the final control signal Vcont for the Lo frequency in a manner similar to the Lo control signal calculating circuit 160 in the first embodiment. The Lo control signal calculating circuit 260 may be implemented by a circuit in the same configuration as the Lo control signal calculating circuit 160. Details on the processing performed by the Lo control signal calculating circuit 260 is omitted to avoid repeating the same description.

As the control signal Vcont is derived from the SP correlation value and outputted from the Lo control signal calculating circuit 260 as described above, the VCO 170 is applied with the control signal Vcont which has undergone a coarse correction for coarse adjustment when the Lo frequency experiences a large shift over an integer number of carriers, and is applied with the control signal which has undergone a fine correction for fine adjustment when the Lo frequency experiences a small shift over a fraction of a carrier. Thus, the Lo frequency can be rapidly and smoothly synchronized to the carrier frequency of the received signal irrespective of the amount of shift in frequency.

The employment of this embodiment as described above enables the error detection both for coarse adjustment and for fine adjustment of the Lo frequency using the pilot signals which are generally inserted in information codes in the OFDM which employs

the synchronous modulation scheme even with the carrier structure that uses SP's as shown in Fig. 19. It is therefore possible to freely set the carrier structure suitable for a particular application without suffering from the positioning of special carriers or restriction on the number of carriers, as required before, in a manner similar to the first embodiment. In addition, the structure of a signal can be advantageously taken into consideration without paying attention to a large restriction on the guard interval length.

Also advantageously, the Lo frequency can be rapidly and smoothly synchronized to the carrier frequency of the received signal irrespective of the amount of shift in the Lo frequency, thereby shortening the pull-in time in the initial synchronization. Further advantageously, the error detection for fine adjustment can be accomplished in a high SN ratio. In addition, in the second embodiment, it is possible to reproduce the synchronization in the time direction for the SP positioning.

Next, a third embodiment of the circuit for detecting a shift in the Lo frequency according to the present invention is illustrated in Fig. 12. The third embodiment is intended for a reduction in circuit scale of the second embodiment.

Specifically, the second embodiment illustrated in Fig. 7 comprises four each of the pilot signal (SP) correlation processing circuits, lower

adjacent signal correlation processing circuits and upper adjacent signal correlation processing circuits, whereas the third embodiment comprises only one each of these circuits. In correspondence, the third embodiment modifies the circuit configuration of the SP position calculating circuit 480, and additionally comprises an SP position generator circuit 490 for calculating and outputting an SP carrier position corresponding to an SP positioning number N_t of a currently received symbol.

Fig. 13 illustrates an exemplary internal circuit configuration of the SP position calculating circuit 480 for use in the third embodiment.

A symbol counter 482 counts up an SP positioning number N_t. A count value N_t outputted from the symbol counter 482 is once latched in a symbol holding circuit 484, and the outputted SP positioning number N_t is held therein for a period in which an effective signal is outputted from the FFT circuit 11.

The SP positioning number N_t outputted from the symbol holding circuit 484 is delivered to the outside of the SP position calculating circuit 480 as the SP positioning number of a currently received symbol.

An SP position protecting circuit 483 is provided for protecting the synchronization established for the cycle of SP positioning. A protection processing procedure performed using this circuit will

be described with reference to a timing chart of Fig. 14. Fig. 14(a) shows a signal at a symbol period outputted from the FFT circuit 11. Each frame represents a symbol, and a number denoted within the frame indicates the SP positioning number Nt'.

On the other hand, Fig. 14(d) shows the SP positioning number N_t outputted from the symbol counter 482. The protection processing described below is performed during a period in which no effective signal exists within each symbol period, for example, during a period of guard interval. During a period in which an effective signal exists, the SP positioning number N_t outputted from the symbol holding circuit 484 is held.

When the SP positioning number is correctly led into synchronization, the SP positioning number (a) of the output signal from the FFT circuit matches the SP positioning number (d) outputted from the symbol counter 482, as can be seen in a left-hand portion of Fig. 14. On the other hand, if the SP positioning number is out of synchronization, the SP positioning number of the output signal from the FFT circuit deviates from the SP positioning number outputted from the symbol counter 482, so that no match is found therebetween, as can be seen in a central portion of Fig. 14. The SP position protecting circuit 483 detects the out-of-synchronization of the SP positioning number using an SP position deviation signal dN_t outputted from the SP position detector

circuit 481. A procedure for calculating the SP position deviation signal dN_t will be described later.

Since the SP position deviation signal dN_t inputted to the SP position protecting circuit 483 represents the difference between the SP positioning number shown in Fig. 14(a) and the SP positioning number shown in Fig. 14(d), the SP position protecting circuit 483 detects that of the SP positioning is out of synchronization when it determines that the $dN_t \neq 0$ stands successively for a predetermined number of symbols. Then, the SP position protecting circuit 483 outputs an SP out-of-sync signal H which indicates that the SP position is out of synchronization. The waveform of the SP out-of-sync signal H is shown in Fig. 14(b).

Turning back to Fig. 13, the SP out-of-sync signal H outputted from the SP position protecting circuit 483 is delivered to the outside of the SP position calculating circuit 480, and inputted to a symbol holding circuit 484.

The symbol holding circuit 484, which has received the SP out-of-sync signal H, is controlled to continue to hold an SP positioning number held at that time for a subsequent symbol period, as shown in Fig. 14(d).

Simultaneously, the symbol holding circuit 484 outputs a load pulse which is delayed by (M_t-1) symbols from the SP out-of-sync signal H, as shown in

Fig. 14(c), which is inputted to a load trigger terminal of the symbol counter 482. The symbol counter 482 is also loaded with the sum (N_t+dN_t+1) of the SP positioning number N_t once held in and outputted from the symbol holding circuit 484 and the SP position deviation signal dN_t. The extra "+1" added in the sum is for counting up the counter.

On the other hand, the symbol holding circuit 484 overwrites the SP positioning number N_t held therein by the loaded value (N_t+dN_t+1) outputted from the symbol counter 482 immediately after the load pulse is outputted in preparation for the operation in the next symbol period. Generally, the SP positioning number synchronization lead-in can be completed in this single protection processing. However, if the SP position is still out of synchronization after the protection processing, the same operation is repeated until the synchronization is pulled in.

With the foregoing protection processing, the SP position calculating circuit 480 in Fig. 12 continues to output the SP carrier position signal corresponding to the SP positioning number of a currently received signal during a normal period in which the SP positioning number is in synchronization. Conversely, when the SP positioning number is out of synchronization, the SP position calculating circuit 480 automatically detects this state, corrects the SP positioning number, and again establishes the

synchronization for the SP positioning number.

The SP position deviation signal dN_t used in the foregoing protection processing is detected by and outputted from the SP position detector circuit 481. Fig. 15 illustrates an exemplary internal circuit configuration of the SP position detector circuit 481.

The SP position calculating circuit 480 in Fig. 12 is supplied with three correlation value signals outputted from an SP correlation processing circuit 410, a lower adjacent signal correlation processing circuit 420, and an upper adjacent correlation processing circuit 430. The three correlation value signals are inputted as they are to the SP position detector circuit 481 in Fig. 13. Referring to Fig. 15 which illustrates the internal configuration of the SP position detector circuit 481, the three correlation value signals inputted to the SP position detector circuit 481 are sequentially loaded into a shift register comprised of flip-flops 610 - 613 in units of symbols. In Fig. 15, a flow of a set of three correlation value signals is represented by a single bold line. Assume also that one frame of flip-flop stores three correlation value signals as one set. Therefore, the shift register stores at all times a total of 12 (=3x4) correlation value signals, which have been calculated from past four symbols.

An SP position selector circuit 620 is provided for calculating the SP position deviation

signal dN_t for leading the SP positioning number into synchronization as described above. The SP position selector circuit 620 is supplied with 12 correlation value signals stored in the shift register comprised of the four flip-flops 610 - 613 to select a symbol which includes a correlation value signal with a maximum amplitude. Then, the SP position selector circuit 620 outputs the value dN_t corresponding to the selected symbol as the SP position deviation signal dN_t.

The SP position selector circuit 620 may output, for example, dN_t equal to zero ($dN_t=0$) when it selects a correlation value signal stored in the flip-flop 610; dN_t equal to 1 or -3 ($dN_t=1$ or -3) when it selects a correlation value signal stored in the flip-flop 613; dN_t equal to 2 or -2 ($dN_t=2$ or -2) when it selects a correlation value signal stored in the flip-flop 612; and dN_t equal to 3 or -1 ($dN_t=3$ or -1) when it selects a correlation value signal stored in the flip-flop 611.

By thus corresponding the value of dN_t to a stored correlation value signal, the value dN_t indicates that the SP positioning number N_t for use in calculating a correlation value for a currently received symbol is deviated by dN_t symbols from the SP positioning number N_t' of a currently received symbol, when the SP positioning number is out of synchronization.

The pull-in of synchronization with this SP

positioning number may be made by using this SP position deviation signal dN_t. It should be noted that if a value (dN_t+1) resulting from adding +1 to the value dN_t is previously corresponded to the SP position deviation signal, the addition of +1 can be omitted when the symbol counter 482 in Fig. 13 is loaded with the SP positioning number.

In the circuit of Fig. 12 having the SP position calculating circuit 480, a coarse adjustment is performed in the following procedure. The description below is made on the assumption that the SP positioning number has already been synchronized.

First, an SP positioning number N_t outputted from the SP position calculating circuit 480 is inputted to the SP position generator circuit 490. Then, the SP position generator circuit 490 calculates an SP carrier position for a symbol corresponding to the inputted SP positioning number N_t for outputting as an SP carrier position signal.

An output signal from the FFT circuit 11 is inputted to the SP correlation processing circuit 410, lower adjacent signal correlation processing circuit 420 and upper adjacent signal correlation processing circuit 430, respectively, which calculate and output three correlation value signals for a currently received symbol under the SP carrier position signal outputted from the SP position generator circuit 490.

Then, the three outputted correlation value

signals are inputted to an error signal calculating circuit 440 for coarse adjustment. The error signal calculating circuit 440 for coarse adjustment calculates and outputs an error signal df_r for coarse adjustment, in a manner similar to the error signal calculating circuit 140 for coarse adjustment in the first embodiment. The error signal calculating circuit 440 may be implemented by a circuit in the same configuration as the error signal calculating circuit 140 for coarse adjustment without modification. Details on the processing performed by the error signal calculating circuit 440 is omitted to avoid repeating the same description.

In this way, the third embodiment is advantageous, similarly to the second embodiment, with respect to the detection of the amount of shift in the Lo frequency in units of the number of carrier rows. The circuit of Fig. 12, however, has a disadvantage in that it takes a longer synchronization lead-in time as compared with the second embodiment since it can synchronizes the SP positioning number only at a cycle of M_t symbols. The third embodiment has another disadvantage in that the SP positioning number cannot be pulled into synchronization if a received level largely varies before and after four consecutive symbols, due to errors occurring in detected SP positioning numbers. Nevertheless, the third embodiment is significantly advantageous in that the

number of correlation processing circuits in Fig. 7 can be largely reduced to significantly reduce the circuit scale.

In Fig. 12, a fine adjustment is performed in the following procedure. In the third embodiment, the error signal calculating circuit for fine adjustment is implemented by the same circuit as the error signal calculating circuit 150 for fine adjustment in Fig. 1. Specifically, a correlation value signal outputted from the pilot signal correlation processing circuit 410 for each symbol is inputted to the error signal calculating circuit 150 for fine adjustment which calculates and outputs an error signal df_d for fine adjustment, in a manner similar to the first embodiment. Details on the processing performed in this event is omitted to avoid repeating the same description.

In this way, the circuit of Fig. 12 can have a similar advantage to the first embodiment in terms of the error detection for fine adjustment in spite of the carrier structure shown in Fig. 19, in which the pilot signals SP are dispersed thereover.

Finally, a summary will be given for a processing procedure for controlling the Lo frequency in Fig. 12. Fig. 16 illustrates an exemplary circuit configuration of an Lo control signal calculating circuit 460 for use in this embodiment.

The circuit of Fig. 16 differs from the circuit of Fig. 6 in that an increased number of items

is provided as selectable in an error signal selector circuit 461. Specifically, when the SP position calculating circuit 480 still outputs the SP out-of-sync signal H, indicating that the SP positioning number is out of synchronization, even after the error signal selector circuit 461 has selected df_r or df_d, the error signal dF for control is set to zero to prevent the Lo frequency from varying. Except for the foregoing, the circuit of Fig. 16 is identical in the manner of operation to the circuit of Fig. 6, so that detailed description on the operation is omitted.

As the control signal Vcont is derived from the SP correlation value and outputted from the Lo control signal calculating circuit 460 as described above, the VCO 170 is applied with the control signal Vcont which has undergone a coarse correction for coarse adjustment when the Lo frequency experiences a large shift over an integer number of carriers, and is applied with the control signal which has undergone a fine correction for fine adjustment when the Lo frequency experiences a small shift over a fraction of a carrier, in a manner similar to the first embodiment. Thus, the Lo frequency can be rapidly and smoothly synchronized to the carrier frequency of the received signal irrespective of the amount of shift in the Lo frequency.

In this way, this embodiment is advantageous, similarly to the second embodiment, with respect to the

detection of the amount of shift in the Lo frequency in units of the number of carriers. This embodiment, however, takes a longer synchronization lead-in time as compared with the second embodiment since it can synchronizes the SP positioning number only at a cycle of M_t symbols. Also, the SP positioning number cannot be led into synchronization if a received level largely varies before and after four consecutive symbols, due to errors occurring in detected SP positioning numbers. Nevertheless, this embodiment is significantly advantageous in that the number of correlation processing circuits in Fig. 7 can be largely reduced to significantly reduce the circuit scale.

It goes without saying that the respective embodiments described above have been illustrated using appropriate circuit configurations which facilitate the description on the basic concepts of the respective embodiments, and that a variety of circuit configurations can be contemplated as having equivalent functions.

For example, in the first embodiment, the circuit scale can be reduced when a complex multiplier circuit and a delay circuit are shared as illustrated in Fig. 17. It should be noted that the circuit of Fig. 1 in the first embodiment separately illustrates the pilot signal correlation processing circuit, upper adjacent signal correlation processing circuit and lower adjacent signal correlation circuit simply for

facilitating the understanding of the description. Also, there are further more kinds of variations contemplated for the circuits of Figs. 7 and 12, such as a shared adder circuit. Since such variations are inexhaustive, description thereon is omitted.

Also, in the respective embodiments described above, the error signal is immediately calculated from the correlation value signal calculated from pilot signals of a currently received symbol in the error signal calculating circuit. However, it is apparent that a similar calculation may be performed after adding and averaging complex vectors of correlation value signals for a plurality of consecutively inputted symbols for further increasing the SN ratio of the correlation value signal.

Particularly, with the carrier structure which uses SP's, since the number of SP carriers to be added is smaller than that of CP carriers, a significant improvement can be made on the SN (CN) ratio when the error signal is calculated not only from the correlation value signal for the currently received and inputted symbol but also from a plurality of added correlation value signals which are calculated from past consecutive symbols.

In the error signal calculating circuit for coarse adjustment, correlation value signals of consecutive symbols may be averaged after their amplitudes have been calculated, instead of the

averaging of complex vectors of correlation value signals, in which case a similar benefit can be provided as well.

Also, the foregoing embodiments have been described on the assumption that a variable range of the Lo frequency is within ±1.5 carriers. However, when the variable range exceeds ±1.5 carriers, the number of the upper adjacent signal correlation processing circuits and the lower adjacent signal calculating circuits may be increased in accordance with the width of the variable range. Then, as will be apparent, a correlation value signal for a carrier at a position in a frequency two carriers lower under a CP carrier or an SP carrier, a correlation value signal for a carrier at a position in a frequency two carriers higher than the same, and so on may be calculated, and amplitude values for these correlation value signals are also compared to select a carrier with a maximum amplitude value.

Preferably, the amplitude value for each correlation value signal is accurately calculated by the following equation:
$\sqrt{[|I|^2+|Q|^2]}$. Alternatively, however, a simplified absolute value may be calculated by $(|I|+|Q|)$ for reducing the circuit scale.

In the addition expressed by Σ_m in the aforementioned equation (1) performed in the correlation processing circuit, some symbols have no

carrier signals to be added in the lower adjacent signal calculating circuit or the upper adjacent signal calculating circuit for CP carriers or SP carriers which exist at the upper end or the lower end of a band. For this reason, the addition expressed by Σ_m in the equation (1) is preferably performed after removing the CP carriers or SP carriers at both ends of the band.

It goes without saying that in the second and third embodiments, the number of removed carriers is the same in all the correlation processing circuit so that the correlation value signals are maintained at the same level.

The foregoing description has been made for embodiments which utilize CP or SP correlation values such that the benefits of the present invention appear clearly. However, similar correlation processing may be performed for TMCC and AC to control the Lo frequency.

Particularly, with the carrier structure using SP's, signals such as TMCC, which have a signal in each symbol, unlike SP, are advantageously free from a problem that four symbols must be awaited in leading the SP positioning number into synchronization. Generally, however, the signals such as TMCC have a smaller number of carriers than that of SP or CP. Therefore, the signals such as TMCC are not preferred due to the inability of largely increasing the SN (CN)

ratio for a resulting error signal and the disadvantage of higher vulnerability to selective fading.

It should be noted that when TMCC or the like is used, the circuit configuration must be designed in consideration of the fact that a phase error exceeding 90 degrees cannot be detected because TMCC or the like is modulated in accordance with DBPSK. Particularly, attention should be paid to the designing of the correlation processing circuit for coarse adjustment.

In the foregoing description, the protecting circuit was treated to the minimum. There are also a large number of variations for a method of inserting the protecting circuit. Since such variations are inexhaustive, description thereon is omitted.

As will be appreciated from the foregoing, the present invention, when employed, eliminates the need for a large number of special carriers having highly randomized positions. For this reason, advantageously, a suitable carrier structure can be freely set for a particular application without paying attention to the positioning of special carriers or restriction on the number of carriers. In addition, since the detection method of the present invention does not use any guard interval, a carrier structure can be advantageously set freely without significant restriction on the guard interval length.

CLAIMS:

1. A signal transmission system of orthogonal frequency division multiplexing having a transmitting apparatus and a receiving apparatus to transmit OFDM signal, said receiving apparatus comprising;

an input portion having an antenna, a mixer and a local oscillator, for receiving said OFDM signal from said transmitting apparatus;

a fast Fourier transforming circuit coupled with said input portion to convert said OFDM signal into base-band signals having a plurality of carriers with a symbol frequency and a predetermined symbol period, said carriers including pilot signals;

a demodulation unit coupled with said fast Fourier transforming circuit, for decoding to be produced as information codes; and

a pilot signal correlation processing unit coupled with said local oscillator and said fast Fourier transforming circuit, for calculating a correlation value relating to said pilot signal, and controlling a frequency of said local oscillator based on the result of calculation of said correlation value.

2. A signal transmission system according to claim 1, wherein said pilot signal correlation processing unit including a calculating circuit for calculating said correlation value between the pilot signal inserted in said carriers of n_S-th (n_S: positive integer) symbol period and the pilot signal inserted in

said carriers of (n-1)-th symbol period.

3. A receiving apparatus in a signal transmission system of orthogonal frequency division multiplexing for transmitting information codes on a plurality of carriers, said carriers being orthogonal to one another and having frequencies different from one another, said receiving apparatus adapted to receive a signal with said carriers having pilot signals inserted therein, said pilot signals being positioned at intervals of a predetermined number of carriers in a frequency axis direction of the carriers of the respective symbols, said receiving apparatus having a local oscillator for generating a locally oscillated signal for frequency converting the received signal, said receiver comprising:

a pilot signal correlation processing circuit for calculating a correlation value signal ΣCP_0 between the pilot signal inserted in the carriers of an n_S-th received symbol in a predetermined frequency and the pilot signal inserted in the same carrier position of an (n_S-1)-th symbol preceding to said n_S-th received signal; and

control means for detecting a phase component of said correlation value signal as an error in frequency of said locally oscillated signal generated by said local oscillator to control a frequency of said locally oscillated signal based on said error.

4. A receiving apparatus according to claim 3,

wherein said control means includes a circuit for controlling the frequency of said locally oscillated signal in a direction in which said error becomes smaller in accordance with a phase angle of said correlation value signal ΣCP_0 in complex vector representation outputted from said pilot signal correlation processing circuit.

5. A receiving apparatus according to claim 3 or 4, further comprising:

a lower adjacent signal correlation processing circuit for calculating a correlation value between a signal on a lower adjacent carrier which is located at least one carrier row below a carrier in which said pilot signal is inserted in said n_S-th symbol of the received signal, and a signal on a lower adjacent carrier of said (n_S-1)-th symbol at the same carrier position as said lower adjacent carrier associated with said n_S-th symbol to output a correlation value signal ΣCP_{-1} in complex vector representation;

an upper adjacent signal correlation processing circuit for calculating a correlation value between a signal on an upper adjacent carrier which is located at least one carrier row above the carrier in which said pilot signal is inserted in said n_S-th symbol of the received signal, and a signal on an upper adjacent carrier of said (n_S-1)-th symbol at the same carrier position as said upper adjacent carrier

associated with said n_S-th symbol to output a correlation value signal ΣCP_{+1} in complex vector representation; and

an error signal calculating circuit for receiving the correlation value signal ΣCP_0 outputted from said pilot signal correlation processing circuit, the correlation value signal ΣCP_{-1} outputted from said lower adjacent signal correlation processing circuit, and the correlation value signal ΣCP_{+1} outputted from said upper adjacent signal correlation processing circuit to calculate an error signal representative of said error based on said correlation value signals.

6. A receiving apparatus in a signal transmission system of orthogonal frequency division multiplexing for transmitting information codes on a plurality of carriers, said carriers being orthogonal to one another and having frequencies different from one another, said receiving apparatus adapted to receive a signal with said carriers having pilot signals inserted therein, wherein said pilot signals are inserted in the carriers at predetermined frequencies at intervals of a predetermined number MT of symbols in the time axis direction, wherein positions of the carriers assigned with said pilot signals are placed with a shift of a predetermined number Mc of carriers in every symbol in a frequency direction, and said pilot signals are inserted at predetermined carrier intervals (McxMt) in the

frequency direction on the carriers of each symbol, said receiving apparatus has a local oscillator for generating a locally oscillated signal for converting a frequency of the received signal into a predetermined frequency, said receiver comprises:

a pilot signal correlation processing circuit for calculating succeedingly correlation values between the pilot signal inserted in the carriers of an n_S-th received symbol in a predetermined frequency and said pilot signal positioned at the same carrier position of an (n_S-Mt)-th symbol located a predetermined number Mt of symbols in front of said n_S-th received signal and calculating a correlation value signal ΣSP_0 which is a sum of the correlation values; and

control means for detecting a phase component of said correlation value signal as an error in frequency of said locally oscillated signal generated by said local oscillator to control a frequency of said locally oscillated signal based on said error.

7. A receiving apparatus according to claim 6, wherein said control means includes an error signal calculating circuit for generating and outputting an error signal indicative of said error based on a phase angle of said correlation value signal ΣSP_0 in complex vector representation outputted from said pilot signal correlation processing circuit.

8. A receiving apparatus according to claim 7, wherein said error signal calculating circuit generates

said error signal indicative of said error using an average value of said current correlation value signal ΣSP_0 in complex vector representation outputted from said pilot signal correlation processing circuit and a plurality of correlation value signals ΣSP_0 calculated from past consecutive symbols.

9. A receiving apparatus according to any one of claims 6 to 8, further comprising:

a lower adjacent signal correlation processing circuit for calculating correlation value between a signal on a lower adjacent carrier which is located at least one carrier row below a carrier in which said pilot signal is inserted in said n_S-th symbol of the received signal, and a signal on a lower adjacent carrier of said (n_S-1)-th symbol at the same carrier position as said lower adjacent carrier associated with said n_S-th symbol to output a correlation value signal ΣSP_{-1} in complex vector representation;

an upper adjacent signal correlation processing circuit for calculating a correlation value between a signal on an upper adjacent carrier which is located at least one carrier row above the carrier in which said pilot signal is inserted in said n_S-th symbol of the received signal, and a signal on an upper adjacent carrier of said (n_S-1)-th symbol at the same carrier position as said upper adjacent carrier associated with said n_S-th symbol to output a

correlation value signal ΣSP_{+1} in complex vector representation; and

an error signal calculating circuit for receiving the correlation value signal ΣSP_0 outputted from said pilot signal correlation processing circuit, the correlation value signal ΣSP_{-1} outputted from said lower adjacent signal correlation processing circuit, and the correlation value signal ΣSP_{+1} outputted from said upper adjacent signal correlation processing circuit to calculate an error signal representative of said error based on said correlation value signals.

10. A receiving apparatus according to claim 9, wherein said error signal calculating circuit includes an error signal calculating circuit for calculating an error signal representative of said error based on the current correlation value signal ΣSP_0 outputted from said pilot signal correlation processing circuit, the current correlation value signal ΣSP_{-1} outputted from said lower adjacent signal correlation processing circuit, the current correlation value signal ΣSP_{+1} outputted from said upper adjacent signal correlation processing circuit, and a plurality of said correlation value signals ΣSP_0, ΣSP_{-1}, ΣSP_{+1} calculated from past consecutive symbols.

11. A receiving apparatus according to any of claims 7 to 10, wherein said pilot signal correlation processing circuit includes:

Mt circuits each for calculating correlation

values between a pilot signal of a currently received symbol and a pilot signal at the same carrier position located Mt symbols in front of the currently received symbol to output a correlation value signal ΣSP_0 in complex vector representation for each of said Mt positioning patterns which differ from one another in positions at which carriers associated with said pilot signals exist; and

a pilot signal position calculating circuit for calculating signals indicative of positions at which carriers exist, said carriers having inserted therein pilot signals in the currently received symbol, based on Mt correlation value signals ΣSP_0 outputted from said pilot signal correlation processing circuit comprising said Mt circuits, to output said signals to said error signal calculating circuit.

12. A receiving circuit according to any of claims 7 to 10, wherein:

said pilot signal correlation processing circuit includes Mt pilot signal correlation processing circuits each for outputting said correlation value signal in complex vector representation for each of said Mt positioning patterns which differ from one another in positions at which carriers associated with said pilot signals exist;

said lower adjacent signal correlation processing circuit includes Mt lower adjacent signal correlation processing circuits each for outputting

said correlation value signal in complex vector representation for each of said Mt positioning patterns;

said upper adjacent signal correlation processing circuit includes Mt upper adjacent signal correlation processing circuits each for outputting said correlation value in complex vector representation for each of said Mt positioning patterns; and

said control means includes a pilot signal position calculating circuit for calculating signals indicative of positions at which carriers exist, said carriers having inserted therein pilot signals within the currently received symbol, based on the Mt correlation value signals ΣSP_0 outputted from Mt pilot signal correlation processing circuits, the Mt correlation value signals ΣSP_{-1} outputted from said Mt lower adjacent signal correlation processing circuits; and the Mt correlation value signals ΣSP_{+1} outputted from said Mt upper adjacent signal correlation processing circuits, to output said signals to said error signal calculating circuit.

13. A receiving apparatus according to any one of claims 7 to 11, wherein said pilot signal correlation processing circuit is a circuit for calculating the correlation value signal ΣSP_0 for a carrier of a pilot signal in the same pilot signal positioning pattern for a period of Mt symbols or more, wherein said receiving apparatus includes a pilot signal position calculating

circuit for receiving said correlation value signal ΣSP_0 outputted from said pilot signal correlation processing circuit to calculate signals indicative of positions at which carriers exist, said carriers having inserted therein pilot signals within the currently received symbol, from the correlation value signal ΣSP_0 of the currently received symbol and correlation value signals ΣSP_0 for Mt symbols previous to the currently received signal, to output said signals to said error signal calculating circuit.

14. A receiving apparatus according to any of claims 7 to 11, wherein said pilot signal correlation processing circuit, said lower adjacent signal correlation processing circuit and said upper adjacent signal correlation processing circuit are circuits for calculating the correlation value signals ΣSP_0, the correlation value signals ΣSP_{-1}, and the correlation value signals ΣSP_{+1} for carriers of the pilot signals in the same pilot signal positioning pattern for a period of Mt symbols or more, wherein said receiving apparatus includes a pilot signal position calculating circuit for receiving said correlation value signals ΣSP_0, ΣSP_{-1}, ΣSP_{+1} outputted from said pilot signal correlation processing circuit, said lower adjacent signal correlation processing circuit and said upper adjacent signal correlation processing circuit, to calculate signals indicative of positions at which the carriers exist, said carriers having inserted therein

the pilot signals within said currently received symbol, from the correlation value signals ΣSP_0, ΣSP_{-1}, ΣSP_{+1} for the currently received symbol, and correlation value signals ΣSP_0, ΣSP_{-1}, ΣSP_{+1} for Mt symbols previous to the currently received signal, to output said signals to said error signal calculating circuit.

15. A receiving apparatus in a signal transmission system of orthogonal frequency division multiplexing for transmitting information codes on a plurality of carriers, said carriers being orthogonal to one another and having frequencies different from one another, as herein described and illustrated in the accompanying drawings.

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Application No: GB 0116263.5
Claims searched: 1 to 15

Examiner: Ken Long
Date of search: 13 February 2002

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.T): H4P (PAL)

Int Cl (Ed.7): H04L 27/26

Other: ONLINE : EPODOC, WPI, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2334836 A	LG ELECTRONICS (page 1 lines 5-9, page 3 lines 13-14, page 4 lines 11-16, page 5 lines 12-16 and page 14 line 13 to page 17 line 1)	1 at least
X	EP 0880250 A1	SONY (page 2 lines 3-4 & 23-27 and page 8 line 47 to page 9 line 46)	1 at least
A	EP 0817418 A1	THOMSON-BRANDT (column 1 lines 3-6 and column 3 line 49 to column 4 line 28)	None
A	WO 99/27671 A1	SAMSUNG (page 1 lines 6-10 & 23-25 and page 2 lines 21-27)	None

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